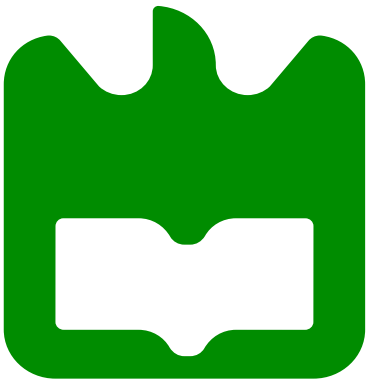
Universidade de Aveiro
Departamento de
Eletrónica, Telecomunicações e Informática
2016

José Miguel
Alves Faria Gomes

Characterization and Modelling of Long-Term Memory Effects in GaN HEMTs

Caracterização e Modelação de Efeitos de Memória Lenta em Transístores GaN HEMT



José Miguel
Alves Faria Gomes

Characterization and Modelling of Long-Term Memory Effects in GaN HEMTs

Caracterização e Modelação de Efeitos de Memória Lenta em Transístores GaN HEMT

Dissertação apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Mestre em Engenharia Eletrónica e de Telecomunicações, realizada sob a orientação científica do Doutor José Carlos Esteves Duarte Pedro, Professor Catedrático no Departamento de Eletrónica, Telecomunicações e Informática da Universidade de Aveiro e sob a co-orientação científica do Doutor Pedro Miguel da Silva Cabral, Professor Auxiliar no Departamento de Eletrónica, Telecomunicações e Informática da Universidade de Aveiro

O júri / The jury

Presidente / President	**Prof. Dr. João Nuno Pimentel da Silva Matos** Professor Associado da Universidade de Aveiro (presidente)
Vogais / Examiners committee	**Prof. Dr. José Carlos Esteves Duarte Pedro** Professor Catedrático da Universidade de Aveiro (orientador)
	Prof. Dr. João José Lopes da Costa Freire Professor Associado com Agregação da Universidade de Lisboa (arguente)

Agradecimentos / Acknowledgements

Quero agradecer em primeiro lugar aos meus pais, José Luís e Margarida Maria, pois sempre me incentivaram e continuam a incentivar a prosseguir os estudos. Quero manifestar também a minha gratidão pelo seu esforço, dedicação e trabalho diários que, sendo o maior exemplo que me puderam dar, permitiram que eu pudesse percorrer o caminho que me trouxe até este momento.

Em segundo lugar, agradeço à minha irmã, Ana Sofia, pelos seus sábios e avisados conselhos e sobretudo porque o seu exemplo é um modelo para mim. Também ao meu cunhado, Luís Rafael, pelo seu exemplo e dedicação. Deixo também um agradecimento especial a duas pessoas que, mesmo não podendo ler este documento, foram, são e serão para mim uma fonte de alegria e motivação, a minha avó, Maria de Jesus, porque foi uma segunda mãe para mim e a minha sobrinha e afilhada, Maria Margarida, pela sua simples existência.

Quero também agradecer a todos aqueles que contribuiram directa ou indirectamente para a realização deste trabalho. Em particular ao professor José Carlos Pedro, pela paixão e sabedoria que evidencia quando transmite o seu conhecimento e experiência, sobretudo a nível técnico-científico, mas não só. Um agradecimento também ao professor Pedro Cabral pela sua co-orientação neste trabalho. Não posso deixar de mencionar também o doutor Luís Nunes e o senhor Paulo Gonçalves, pelas opiniões e sugestões que me ofereceram durante a execução do trabalho experimental.

Por fim, uma palavra especial para todos aqueles que encontrei ou re-encontrei durante a conclusão deste trabalho no Instituto de Telecomunicações. Muito obrigado a todos pelo apoio.

Palavras-chave

"Drain-Lag", "Gate-Lag", Transístores de Nitreto de Gálio, Efeitos de Memória Lenta, Medidas Pulsadas I-V, Modelação de Transístores, Efeitos de Armadilhamento de Electrões

Resumo

A tecnologia GaN HEMT tem revolucionado o mercado dos amplificadores de potência para RF. O seu potencial, comparado com tecnologias anteriores, como a Si LDMOS, continua por ser completamente explorado. Contudo, a falta de uma boa caracterização e modelação dos efeitos de memória lenta causados pelo armadilhamento de cargas têm impedido o total aproveitamento desta tecnologia no desenho de amplificadores de potência. Consequentemente, estes fenómenos de armadilhamento têm sido alvo de um amplo estudo tanto a nível científico como industrial. Isto deve-se, sobretudo, porque a linearidade dos amplificadores baseados nesta tecnologia é bastante afectada pelo estado de armadilhamento de cargas no dispositivo, que, por sua vez, é definido pela tensão de pico na saída, *drain*, do transístor. As ferramentas de desenho de circuitos auxiliado por computador estão presentes na maioria dos laboratórios de investigação. No entanto, estas dependem não só dos seus algoritmos de simulação mas também, em larga medida, dos modelos nelas utilizados, tornando fundamental o desenvolvimento de melhores modelos.

O presente documento descreve a extracção de um modelo de circuito equivalente de pequeno signal dependente da polarização, de um transístor GaN HEMT de 3.3 W, a partir de medidas de parâmetros-S pulsadas, assim como a construcção de um sistema de medidas pulsadas *DC I-V* e a utilização deste último na caracterização de efeitos de armadilhamento. O sistema desenvolvido, baseado em dois circuitos pulsadores desenhados para medidas pulsadas quer no terminal de entrada, *gate*, quer no de saída, *drain*, foi automatizado através do software MATLAB instalado num PC. Os circuitos pulsadores permitem larguras de pulso na escala dos microsegundos com *duty-cycles* tão pequenos como 0.001%, assim como, elevadas tensões de saída - perto de 50 V - e correntes - pelo menos até 4 A. Com o sistema desenvolvido, obtiveram-se curvas I-V iso-térmicas e também curvas I-V iso-dinâmicas, dependentes do estado de armadilhamento, de um transístor GaN HEMT de 15 W. De modo a obter as últimas, foram utilizadas medidas de duplo-pulso. A assimetria esperada nas constantes de tempo associadas com o *drain-lag* foram claramente observadas: na escala dos ns para o armadilhamento e das centenas de milisegundos para o desarmadilhamento. Tal como a literatura prevê para tecnologias mais recentes de GaN HEMTs, o impacto dos fenónemos de *gate-lag* que foi observado revelou-se bastante reduzido.

Keywords Drain-Lag, Gate-Lag, GaN HEMT, Long-Term Memory Effects, Pulsed I-V Measurements, RF Transistor Modelling, Electron Trapping Effects

Abstract

Gallium nitride (GaN) high electron mobility transistor (HEMT) technology has been revolutionizing the RF power amplifier (PA) market. Its potential, versus existing technologies, such as Silicon (Si) Laterally-Diffused MOS(LDMOS), is yet to be completely explored. However, the lack of good characterization and modelling of charge carrier trapping related phenomena has been hampering PA designers from extracting this technology's promised performance. Hence, GaN HEMT trapping has been given a great amount of attention by the scientific and industrial worlds. This is mainly because the overall linearity of the PA built with this technology is affected, to a great extent, by the trapping state dependence on the device's drain peak voltage. Circuit computer-aided design (CAD) tools are almost ubiquitous at research and development labs. However, these tools rely, not only on their simulation algorithms, but also on their built-in device models. This makes the development of accurate models a fundamental task.

This work reports a multi-bias small-signal equivalent circuit (SSEC) model extraction procedure of a 3.3 W GaN HEMT from pulsed S-parameters as well as the development of a pulsed DC I-V measurement system and its use in the characterization of trapping-effects. This system, which is based on two pulser circuits, designed specifically for gate and drain pulsed measurements, was then automated through a MATLAB/PC controller. The pulser circuits allowed pulse widths on the microsecond scale at very low duty cycles as well as high peak voltages - close to 50 V - and currents - up to 4 A. With the developed system, isothermal standard pulsed I-V curves, as well as trapping-state dependent, isodynamic, pulsed I-V curves were obtained from a 15 W GaN HEMT device. In order to obtain the latter, the so-called double-pulse measurement technique was used. The expected asymmetric time constants associated with drain-lag were clearly observed: on the ns scale for the trapping and on the hundreds of milliseconds for the de-trapping. The predicted relatively reduced impact of gate-lag phenomena in more recent GaN HEMT technologies was also verified.

Table of Contents

Table of Contents i

List of Figures iii

List of Tables ix

List of Acronyms and Symbols xi

1 Introduction 1

1.1 Wireless Telecommunications and the Power Amplifier 1

1.2 Modern RF Power Transistor Technologies 4

1.3 RF Power Transistors Modelling 5

1.4 Pulsed DC I-V and Trapping Related Long-term memory effects (LTME) 7

1.5 Dissertation Objectives 9

1.6 Dissertation Outline 9

2 RF Power Transistors Modelling 11

2.1 DC Modelling: I-V Curves 14

2.2 Small-Signal Equivalent Circuit: SSEC 15

2.3 Extending the Model to Large-Signal 21

2.3.1 Multi-Bias Linear Models 21

2.3.2 Non-linear Models 23

2.4 Model Enhancements 26

2.4.1 Thermal Effects 27

2.4.2 Gate-Source Diode 28

2.4.3 Voltage Breakdown Modelling 29

3 Pulsed I-V System Design and Implementation 31
3.1 Pulsed I-V/RF Systems Overview . . . 31
3.1.1 Pulsed Measurements . . . 32
3.1.2 Commercial Pulsed Measurements Systems . . . 32
3.1.3 Pulsed Measurement Systems Reported in Literature . . . 34
3.1.4 Laboratorial Pulsed I-V System . . . 36
3.2 Gate Pulser . . . 37
3.3 Drain Pulser . . . 42
3.4 Pulsed I-V Measurement System . . . 50
3.4.1 DUT Testbed . . . 50
3.4.2 Pulsed DC Bias-Tees . . . 51
3.4.3 SMA/DC Cables . . . 52
3.4.4 Measurement Setup Diagrams . . . 53
3.4.5 Data Acquisition and Processing . . . 55

4 GaN HEMT LTME due to Trapping 57
4.1 What are LTME? . . . 57
4.2 Trapping Effects in GaN HEMTs . . . 61
4.3 Pulsed Gate I-V Measurements: Gate-Lag . . . 65
4.3.1 Single-Pulse IV-Curves . . . 65
4.4 Pulsed Drain I-V Measurements: Drain-Lag . . . 68
4.4.1 Single-Pulse IV-Curves . . . 69
4.4.2 Double-Pulse - *Quasi-Isodynamic* - IV-curves . . . 71
4.5 Modelling Trapping Related LTME . . . 73
4.5.1 Including Trapping Related LTME in Compact Models . . . 73
4.5.2 Trapping State Dependent Threshold Voltage: V_T Model . . . 76

5 Conclusion and Future Work 79
5.1 Conclusion . . . 79
5.2 Future Work . . . 80

Bibliography 81

Appendix A *Agilent ADS* Simulation Schematics 89

Appendix B PCB Layouts 91

List of Figures

1.1 Evolution of wireless telecommunications, reprinted from [1]. 2
1.2 A general modelling design abstraction level hierarchy, reprinted from [13]. . . . 6
1.3 Measurements from which the non-linear transistor compact model parameters are extracted. 7
1.4 Pulsed I-V measurement waveform shape and sampling time window representation. 8

2.1 Qualitative comparison between different RF PA modelling approaches, adapted from [15]. 12
2.2 Modelling procedure flowchart, reprinted from [17]. 13
2.3 Typical DC I-V curves of a FET highlighting different typical characteristics of these devices, reprinted from [18]. 15
2.4 Small signal equivalent circuit topology, SSEC, adapted from [18]. 17
2.5 RF power transistor plastic and ceramic packaging examples, reprinted from [13]. 17
2.6 Intrinsic parameters versus frequency obtained at $V_{DS} = 15$V and $V_{GS} = -2.3$ V for a 3.3 W GaN HEMT. 20
2.7 SSEC ADS schematic used for comparison with S-parameter measurement data of a 3.3 W GaN HEMT. 21
2.8 Comparison between model and measurements from 500 MHz to 10 GHz. 22
2.9 Comparison between model and measurements from 500 MHz to 10 GHz under the 'cold-FET' condition ($V_{DS} = 0$ V), at $V_{GS} = -4$ V (cut-off) and $V_{GS} = 2$ V (forward bias). 22
2.10 SSEC extracted C_{gs} versus V_{GS} for $V_{DS} = 0$ V to $V_{DS} = 100$ V. 23
2.11 Extracted SSEC g_m versus V_{GS} for $V_{DS} = 0$ V to $V_{DS} = 100$ V. 24
2.12 Temperature effect on a pHEMT, reprinted from [18]. 27

2.13 Thermal RC sub-network of the equivalent-circuit thermal model used to calculate current degradation from average dissipated power, reprinted from [13]. . . 28
2.14 Breakdown mechanisms in a general GaN HEMT, reprinted from [11]. 29

3.1 Commercial pulsed I-V systems. Left: Agilent (now Keysight) Power Device analyser/Cruve Tracer, reprinted from [31]. Right: Maury Microwave/AMCAD Engineering pulse I-V system, reprinted from [17]. 32
3.2 Specifications for several pulser heads available from Auriga Microwave, reprinted from [32]. 33
3.3 Pulsed I-V header options. Left: Standalone pulser head adaptor from Auriga Microwave, reprinted from [32]. Right: Modular pulsed I-V heads from Focus Microwaves, reprinted from [33]. 33
3.4 Pulsed I-V instrument architecture diagram, reprinted from [38]. 35
3.5 Pulsed I-V and the connection between DUT and the instrumentation, reprinted from [40]. 36
3.6 Schematic of the new pulsed measurement system, reprinted from [42]. 36
3.7 Gate pulser circuit schematic. 39
3.8 Gate pulser simulations with a GaN HEMT model biased at $V_{DS} = 28$ V used as load. Left: input and output voltage pulses. Right: output voltage and current pulses. 40
3.9 Gate pulser PCB implementation. 40
3.10 Gate pulser response to 1 µs input pulses with 200 ns rise time. Left: No load, i.e., open output. Right: Loaded with a 120 pF capacitor. 41
3.11 Gate pulser response to 1 µs input pulses with 200 ns rise time exciting a 15 W GaN HEMT gate. Left: Output voltage. Right: Output current. 41
3.12 Drain pulser circuit schematic. 43
3.13 Drain pulser output stage circuit schematic. 47
3.14 Drain pulser simulation input and output voltage pulses. Left: 10 Ω load resistor. Right: 15 W GaN HEMT model biased at $V_{GS} = 0$ V DC. 48
3.15 Drain pulser simulation output voltage and current pulses. Left: 10 Ω load resistor. Right: 15 W GaN HEMT model biased at $V_{GS} = 0$ V DC. 48
3.16 Drain pulser PCB implementation. 49
3.17 Drain pulser response to a 10 µs pulse loaded with a 12 Ω resistor. Left: Output voltage. Right: Output current. 50
3.18 DUT test-bed. 51

3.19 Left: Aeroflex/INMET 8860S pulsed bias-tee. Right: pulsed bias-tee DC to RF+DC and AC to RF+DC insertion loss, reprinted from [44]. 51
3.20 Current probe, TCP0030, clamped to the modified coaxial cable. 52
3.21 Setup diagram for pulsed I-V curves extraction using the gate pulser. 53
3.22 Setup diagram for pulsed I-V curves extraction using the drain pulser. 54
3.23 Pulsed I-V measurement setup implemented at the Telecommunications Institute RF laboratory. 54
3.24 Close-up view of the test-bed and drain-pulser when performing measurements. 55
3.25 Example of a pulsed I-V measurement temporal diagram. 56

4.1 Long and short-term memory effects sources in a transistor circuit, adapted from [49]. 58
4.2 Dispersion in the AM-to-AM and AM-to-PM curves from a 400 W Doherty PA using a wideband code-division multiple access (WCDMA) signal. Blue: Measured, Red: Modeled, reprinted from [52]. 59
4.3 Representative current response when voltage pulses of different time widths are applied at the gate or drain terminal of an RF FET, reprinted from [53]. 60
4.4 GaN HEMT simplified physical structure, reprinted from [56]. 61
4.5 Trapping causes representation in GaN HEMTs, reprinted from [57]. 62
4.6 Comparison of HEMT structures: conventional HEMT versus an HEMT with a recessed-gate surface structure, reprinted from [12]. 63
4.7 Knee-walkout and current collapse effect on optimum load-line for maximum output power in GaN HEMTss, reprinted from [62]. 64
4.8 Gate-lag process representation in a GaN HEMT, reprinted from [65]. 65
4.9 Exemplary voltages at gate and drain measured for the I-V curves of a 15W GaN HEMT, the values extracted correspond to the average of the samples with red circles: 13 μs to 14 μs. 66
4.10 Different sampling windows used during pulsed gate measurements in the triode region. Black circles: 1 μs to 2 μs after the pulse rising edge. Red circles: 8 μs to 9 μs after the pulse rising edge. 66
4.11 I-V curves obtained using the different sampling windows shown in Figure 4.10, blue curves correspond to black dotted sampling window and the red curves to the red dotted window. 67

4.12 Gate pulsed I-V curves obtained, inside the red circle the negative slope of the curves reveal thermal effects within the 5 μ s and/or trapping drain related trapping. 68
4.13 Charge carrier trapping due to high drain voltages resulting in the drain-lag effect, a) and b) reprinted from [11], c) from [66]. 69
4.14 Pulsed V_{DS} and the resulting I_{DS} with the sampling windows used marked with red circles: 17 μs to 19 μs, after the voltage pulse rising edge. 70
4.15 Typical I_{DS} and V_{DS} time-domain waveforms resulting from drain-pulsed measurements. 70
4.16 Pulsed measurement transients due to trapping of charge carriers in a 15 W GaN HEMT. Blue trace(Step Up): $V_{GSq} = 0$ V, $V_{DSq} = 0$ V and $V_{DS,peak} = 30$ V; Red trace(Step Down): $V_{GSq} = -3.6$ V, $V_{DSq} = 18$ V and $V_{DS,peak} = 28$ V, reprinted from [67]. 71
4.17 Double pulsed V_{DS} and the resulting I_{DS} with the sampling windows used marked with red circles: 17 μs to 19 μs, after the voltage pulse rising edge. The pre-pulse was of $V_{DS} = 10$ V and the gate quiescent voltage was $V_{GSq} = -3$ V. 72
4.18 I-V curves acquired with the double pulse measurement technique for a 15 W GaN HEMT. Blue trace: $V_{DSq,pre} = 10$ V; Red trace: $V_{GSq,pre} = 45$ V. 72
4.19 I-V curves acquired with the double pulse measurement technique using different pre-set voltage pulses for a 15 W GaN HEMT. 73
4.20 Enhanced EEHEMT1 model with circuit elements describing gate and drain lag effects, reprinted from [57]. 74
4.21 Schematic of the drain-lag equivalent-circuit model, reprinted from [70]. 75
4.22 Different I-V plots resulting from the double-pulse measurement with different pre-set pulses of: 10 V, 20 V, 30 V and 45 V. Measured data is drawn in black, blue crosses represent the data used for the fitting of the models and the resulting fitted models are drawn in red. The resulting model parameters are forced to be the same in all the models/graphs except the threshold voltage which is allowed to vary for each pre-pulse voltage, i.e., each graph's red traces represent a different model but just due to the different V_T resulting from each fit. 76
4.23 Extracted threshold voltage versus the V_{ds} pre-pulse voltage, reprinted from [67]. 77

A.1 Gate pulser *Agilent ADS* simulation schematic. The blocks corresponding to the device models used were obtained from the manufacturer. 89

A.2 Drain pulser *Agilent ADS* simulation schematic. The blocks corresponding to the device models used were obtained from the manufacturer. 90

B.1 Layout of the gate pulser PCB implementation on an FR-4 substrate. 91
B.2 Layout of the drain pulser PCB implementation on an FR-4 substrate. 92

List of Tables

1.1 Semiconductor material properties, reprinted from [9]. 4

2.1 Common commercial models for GaN HEMTs, adapted from [16]. 12
2.2 Extracted extrinsic parameters for a 3.3 W GaN HEMT. 18
2.3 Extracted intrinsic parameters at $V_{DS} = 15$ V and $V_{GS} = -2.3$ V for the 3.3 W GaN HEMT. 20

3.1 Power OpAmp PB63 pin use and description. 44

List of Acronyms and Symbols

2DEG Two-dimensional electron gas

AC Alternate current

ADS Advanced Design System

Al_2O_3 Sapphire

AM-to-AM Gain compression

AM-to-PM Phase transfer characteristic

AWG Arbitrary waveform generator

AlGaN Aluminium gallium nitride

BJT Bipolar junction transistor

CAD Computer-aided design

DC Direct current

DUT Device under test

EER Envelope elimination and restoration

EM Electromagnetic

ET Envelope tracking

FET Field-effect transistor

GPIB General Purpose Interface Bus

GaAs Gallium arsenide

GaN Gallium nitride

HEMT High electron mobility transistor

HPA High power amplifier

ICCAP Integrated Circuit Characterization and Analysis Program

IC Integrated circuit

IF Intermediate frequency

III-V 3^{rd} and 5^{th} row semiconductor elements of the periodic table

IMD3 Third-order IMD

IMD Inter-modulation distortion

IR Infra-red

IoT Internet of things

LAN Local area network

LDMOS Laterally diffused MOSFET

LED Light-emitting diode

LTME Long-term memory effects

LUT Look-up table

M2M Machine-to-machine

MATLAB Matrix Laboratory

MESFET Metal-semiconductor FET

MET Motorola electro thermal model

MIMO Multiple-input and multiple-output

MMIC Monolithic microwave integrated circuit

MOSFET Metal-oxide-semiconductor FET

OFDM Orthogonal frequency-division multiplexing

OpAmp Operational amplifier

PAPR Peak to average power ratio

PA Power amplifier

PAE Power-added efficiency

PCB Printed circuit board

PC Personal computer

pHEMT Pseudomorphic HEMT

QAM Quadrature-amplitude modulation

RF Radio-frequency

SMA Sub-miniature version A

SNR Signal to noise ratio

SSEC Small-signal equivalent circuit

Si Silicon

SiC Silicon carbide

$\mathbf{Si}_x\mathbf{N}_x$ Silicon nitride

TCAD Technology CAD

TWTA Travelling-wave tube amplifier

VXI Versa Module Europa (VME) eXtensions for Instrumentation

WCDMA Wideband code-division multiple access

WLAN Wireles local area network

Chapter 1

Introduction

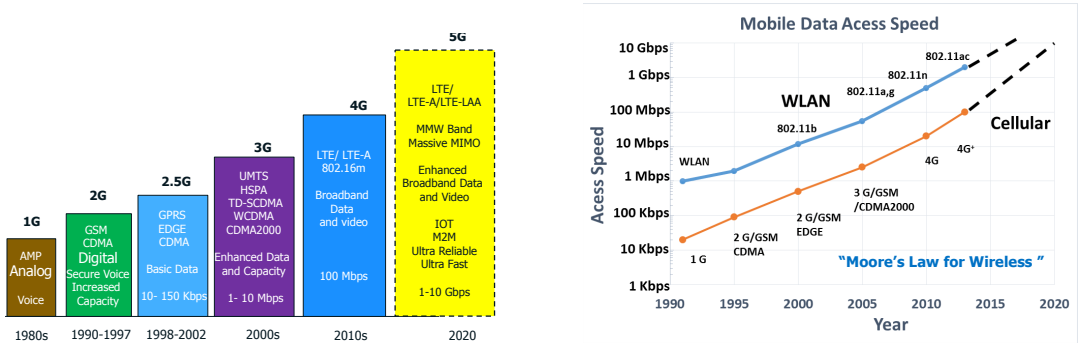
1.1 Wireless Telecommunications and the Power Amplifier

Telecommunications are still one of the most technology hunger fields. Despite its early times have addressed almost only military and defence applications, nowadays, both civil and military applications are big driving forces in this ever bigger market. Regarding wireless civil applications the main advantages offered by this technology are mobility, portability and ease of connection. All these advantages are possible due to the controlled emission and reception of electromagnetic (EM)-waves. The theoretical framework behind this branch of science is deeply associated with the work of Maxwell and saw first real usage when Heinrich Hertz developed an oscillator. Hertz studied and created radio waves using a dipole, reason why this early type of antenna is often named the Hertz dipole.

The first transatlantic point-to-point communication link is attributed to Guglielmo Marconi, in 1901, and, surprisingly, it was digital! In fact, the first signals transmitted were telegraph signals, which are more of a digital rather than analogue nature. Nevertheless, telecommunications were already used before Maxwell, Hertz and Marconi. Going back in time, wired electrical telegraphy was already a mature and well-deployed technology by the time of the first production of EM waves. Even before electrical wired telegraphy, smoke signals, optical beams or reflected light were already used as means of communication at long distances in the 1700's and 1800's.

Commercial wireless telecommunications are today a huge market of billions of €'s. It started to grow significantly on the 1980's with the development of the cell phone. On the 1990's, the use of wireless telecommunications for personal usage lead to an exponential growth with two big areas spawning, cellular telecommunications and wireless data networks.

Cellular telecommunications are grouped in generations: 1G, 2G, and so on. The first generation transitions occurred due to technological breakthroughs or big changes in the employed paradigm. Nowadays, however, the birth of new generations is more often related to market and economical reasons rather than to big technological breakthroughs. Figure 1.1 shows a comparison of the already established 4 generations of cellular telecommunications plus the forthcoming 5^{th} generation, as well as a comparison between the wireless and cellular access speeds evolution over time.



(a) Cellular telecommunications evolution by generations.

(b) Wireles local area network (WLAN) and cellular access speed over time.

Figure 1.1 Evolution of wireless telecommunications, reprinted from [1].

Access speeds kept increasing at a growing pace for both WLAN and cellular until the present days and are expected to keep on growing in the near future. The 5^{th} generation will bring some technical novelties such as the usage of millimetre-waves and Massive-multiple input and multiple output (MIMO), among others. These and other developments are expected to allow for the dissemination of machine-to-machine (M2M), internet of things (IoT) and increase the speed, amount and reliability of data transmission.

Radio-frequency (RF) PAs are one of the most important parts of the wireless infrastructure. Their purpose is to feed the antennas with sufficiently powerful RF signals such that these can be radiated and reach the receiver RF antenna/front-end at enough power levels. Given that the EM-waves get dispersed as they travel, at least proportionally to the square of distance, the most obvious way to overcome the channel attenuation is to radiate more power. If sufficient power is received, the data sent through these signals can be recovered. Generating more power at high frequencies is not trivial though, at least without either doing that in a very inefficient way in terms of energy or using, unintentionally, more spectrum than the one actually needed due to non-linearities. In fact, due to the non-linearities inherent to these

devices, inter-modulation distortion (IMD) and spectral regrowth will arise, meaning that a relevant amount of power will be radiated at undesirable frequencies, being the most problematic the ones adjacent to the frequency band/(s) being used. Actually, the latter problem gets more complicated as EM-spectrum regulators do not even allow the deployment of Power amplifiers (PAs) which contaminate the spectrum, not allocated to its intended applications, beyond a certain power level. The paradigm being discussed so far is usually short-termed as the well known linearity-efficiency compromise [2, 3].

RF PAs are usually sub-divided in classes according to their operation regime. Class-A PAs are the least-efficient and most linear class. There are many other classes, such as: B, C, D, E, F, as well as more involved topologies like the Chireix, Doherty, envelope tracking (ET) and envelope elimination and restoration (EER) [4–8]. Classes which are more energy efficient tend to be more non-linear as well. The non-linearities have a big impact on today's wireless telecommunication signals that include amplitude modulation together with frequency modulation, such as, orthogonal frequency division multiplexing (OFDM) and quadrature-amplitude multiplexing (QAM). Moreover, the signals mentioned before typically have high peak to average power ratios (PAPRs), i. e., the input signal may be at lower power levels during most of the time but there will be high power peaks occasionally. Thus, having in mind that PAs are more efficient when they operate closer to saturation but also that they need to withstand the signal peaks without producing too much distortion, they are usually set to work at a given back-off power, augmenting even more the efficiency problem.

When designing the PAs that will be used in base stations, it is desirable to have the most accurate and reliable models of the electronic components that will be used. The more accurate the models used within computer-aided design (CAD) simulation software, the more accurate will be the final power amplifier (PA) implementation measured metrics when compared to the simulated ones. Furthermore, control circuitry and pre-distortion circuits become easier to design and their real implementation will be more predictable. This may ultimately lead to a first-pass design or, at least, fewer iterations will be necessary in order to meet the required specifications. New device technologies bring new possibilities and but also new challenges. It is therefore crucial to study and characterize these new devices and provide circuit designers with the most accurate and complete models, exposing their advantages but also their faults. This is of paramount importance for the main component of solid-state PAs, the transistor.

1.2 Modern RF Power Transistor Technologies

Wireless telecommunications, are, nowadays, intimately related to transistor device developments. More recently, wide band-gap technologies such as gallium nitride (GaN) high electron mobility transistor (HEMT) appeared. Given their relative infancy, these keep being developed or improved to fulfil size, weight, power and cost demands. Therefore, transistor and other semiconductor devices and their associated technologies continue to be a major area of research and development.

GaN materials started revealing as a promising solution for high power/frequency applications in the early 90's, [9]. Their main advantages are, among others, the higher saturated electron velocity and electron mobility, which allow higher frequency operation, as well as a wider band-gap allowing for higher breakdown fields, which translates in higher breakdown voltages and higher output powers. Table 1.1 shows a comparison of the principal properties of semiconductor technologies typically used in RF power transistors.

Semiconductor (Typical Materials)		Silicon	Gallium Arsenide	Indium Phosphide	Silicon Carbide	Gallium Nitride
Characteristic	Unit					
Bandgap	eV	1.1	1.42	1.35	3.25	3.49
Electron Mobility at 300 °K	cm^2/Vs	1,500	8,500	5,400	700	1,000–2,000
Saturated Electron Velocity	$\#10^7$ cm/s	1	1.3	1	2	2.5
Critical Breakdown Field	MV/cm	0.3	0.4	0.5	3	3.3
Thermal Conductivity	W/cm °K	1.5	0.5	0.7	4.5	>1.5
Relative Dielectric Constant	ε_r	11.8	12.8	12.5	10	9

Table 1.1 Semiconductor material properties, reprinted from [9].

From the semiconductor physical characteristics presented in Table 1.1, it is clear that GaN has great advantages when compared to other technologies. However, due to their maturity, good performance and lower costs, silicon (Si) bipolar junction transistor (BJT) and laterally-diffused metal-oxide semiconductor (LDMOS) are major competitors of GaN HEMTs in the aerospace and defence markets and, the latter, in commercial base-stations. When very high power is needed, vacuum devices, such as travelling-wave tube amplifier (TWTA), are still preferred, although GaN HEMTs are starting to take their place as this technology matures and its costs become lower. The numbers in Table 1.1 can be translated to more familiar PA terms such as higher power-densities due to the increased operating voltage, consequence of the wider band-gap, and current, due to higher carrier concentration. Furthermore, higher

frequencies are possible, due to the increase in mobility and saturated velocity of electrons, especially when compared to Si LDMOS.

GaN development was greatly accelerated by the pursuit of the blue and white light-emitting diodes (LEDs). In the early 1990's, the two-dimensional electron gas (2DEG) was observed at the aluminium gallium nitride (AlGaN) hetero-junction, [10]. The formation of that electron sheet has the advantage of replacing doping techniques used in other technologies which introduced impurities and consequently reduced the mobility of carriers [11]. The piezoelectric characteristics of GaN material lead to higher current densities when compared with field-effect transistors FETs using Si and gallium arsenide (GaAs), the 2DEG generated can be 10 times bigger, thus increasing the current density [12]. However, there are some less positive aspects about GaN too, the first is that there are still no GaN substrates and typically Si, silicon carbide (SiC) or sapphire (Al_2O_3) are used, all of them with their advantages and disadvantages. Furthermore, GaN thermal conductivity does not follow the power density increase and may limit the maximum power achievable in practice. There is also a negative aspect about the piezoelectric behaviour of the device, high fields can cause structural damage due to mechanical stress which can affect the reliability of the technology.

One of the most important causes for the lack of accuracy between simulations and measurements of GaN based RF PAs is the trapping of charge carriers. These phenomena has drawn a considerable amount of attention from researchers and industry at both the device physics and production levels. Furthermore, it is a relevant topic in the RF modelling and PA design fields. Without getting too much into the physics and device production sides, RF engineers and modellers need to focus on the accurate characterization and understanding of these mechanisms so that they can be properly studied and modelled and their impact accurately predicted and/or mitigated.

1.3 RF Power Transistors Modelling

Modelling of RF components is a necessary step in order to fully exploit the power of circuital simulators. Without proper models, the practical impact of these software tools would be much more limited. Modelling active devices, such as transistors, can be a reasonably difficult task, at least within decent limits of usability, size and ease of extraction from the measurements one can obtain from these devices. Therefore, several modelling approaches and extraction methodologies are used, such as, behavioural and compact models.

High power amplifiers (HPAs) design has become more complex in terms of competing

multi-dimensional parameters such as bandwidth, efficiency, linearity and power. The behaviour of these devices can be very different under large-signal conditions than for small-signals. Furthermore, electro-thermal effects are often a critical issue and require isothermal measurements or other temperature controlled characterization. Moreover, emerging wireless technologies use more complex digital modulations which brings new challenges in the modelling and design processes.

A modelling abstraction level hierarchy is depicted in Figure 1.2. At the lower abstraction levels there are the physics based models, which are seeing increased use, namely in the technology development iterations, in what is called technology CAD (TCAD). Then we have compact models, that bridge the physics of the device into equivalent circuits, amenable to be integrated in circuit simulator where Kirchhoff's current and voltage laws are used. The physical meaning of the parameters may be lost though, but the complexity and simulation time is greatly reduced. Behavioural models, lie at a fairly high level of abstraction but they are becoming more valuable as the need for digital pre-distortion increases and therefore, computationally efficient and fast to extract system/circuit models are required.

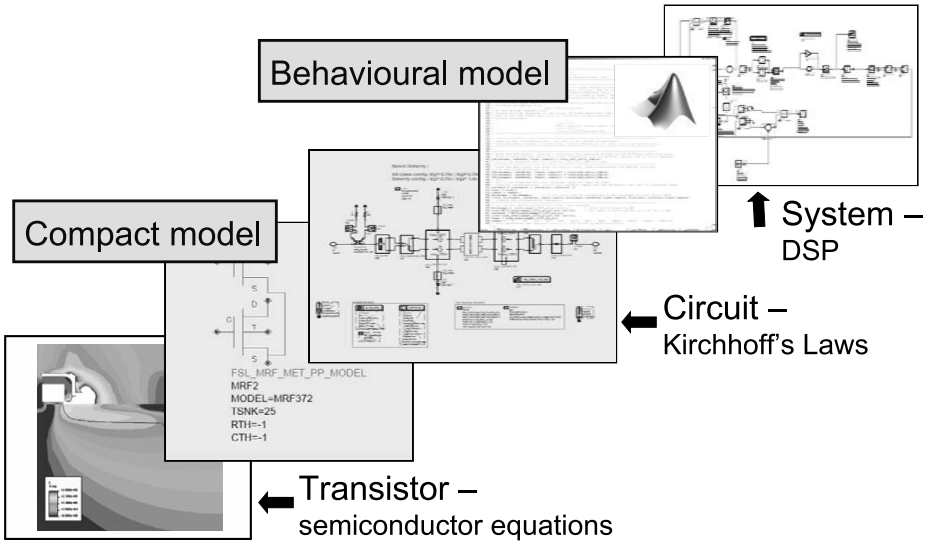


Figure 1.2 A general modelling design abstraction level hierarchy, reprinted from [13].

Compact models are very often used at the device level, these rely on an equivalent linear circuit topology or "template", which is appropriately selected or developed for the technology/device to be modelled. Besides the linear elements, analytical expressions for the non-linear components such as capacitances, current-sources, diodes, etc. are used as well. To extract these parameters, more than one measurement type is recommended. Figure 1.3 shows which measurements are typically used to extract the different compact model parameter

types from. The overlapping of different type of measurements used to extract the same parameters can be observed, which means that different measurements can be used to extract the same parameters and validate each other. The non-linear active components such as the current source, need to be consistent in all of the measurements space. However, electro-thermal and trapping effects are only observable and thus extractable when the device is driven with sufficiently powerful signals such that the device temperature or trapping state changes. Recent trends in device modelling for circuit design, including PA design, tend to use compact models together with electromagnetic simulations, due to the ever increasing shift upwards in the frequency spectrum.

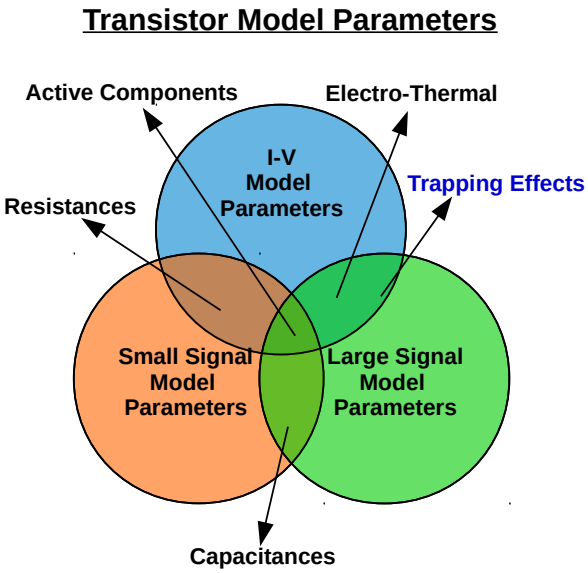


Figure 1.3 Measurements from which the non-linear transistor compact model parameters are extracted.

1.4 Pulsed DC I-V and Trapping Related LTME

The actual RF operating conditions are often not attainable at the measurement environment, either due to current/voltage/power constraints or the limitation in pulse widths of pulsed measurements. Nevertheless, several types of measurements can, or need to, be used in order to obtain an accurate model of an RF power transistor. Direct current DC measurements are important to model the device's current-source voltage dependence but they may heat-up the device and ultimately destroy it. Therefore, I-V graphs are typically drawn from

pulsed measurements, called pulsed DC I-V. The used pulses are too long to be considered in the RF range, and that is why they are called DC, even though they are obtained from pulsed excitations. Moreover, these type of pulsed excitation may be used to bias the device and thus allow the measurement of bias-depend pulsed S-parameters which are desirable at any FET or HEMT compact modelling process.

Although very important for the characterization of transistor devices, pulsed measurements can be very useful as well in the observation and characterization of long-term memory effects (LTME) related to either temperature, bias-networks or electron trapping. The figures of merit of GaN HEMT based PAs resulting from computer simulations are often too far from what is measured of their real implementation. One of the reasons for that is the limited modelling of LTME which prevents the prediction of the negative impact these effects have on the overall circuit implementation. Thus, in this work, pulsed measurements were aimed at the characterization of LTMEs, particularly caused by the trapping phenomena.

Figure 1.4 shows a general pulsed excitation waveform and the sampling windows and durations one may choose. To obtain isothermal I-V curves it is important to use, not only a low duty cycle but also a narrow pulse. However, if it is too narrow the sampling window falls into the transient response and the resulting measurements become less reliable.

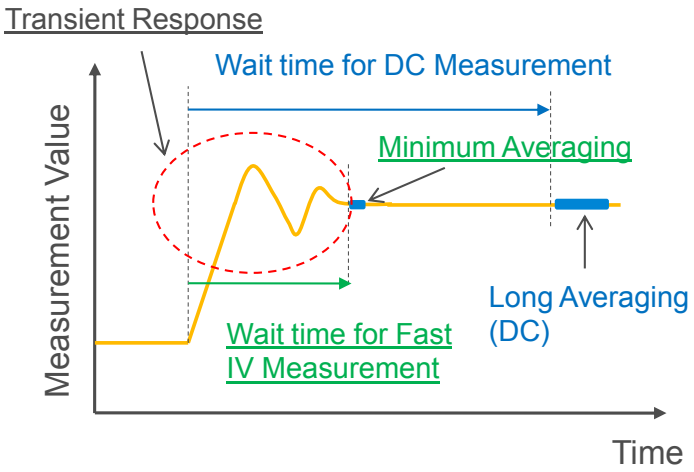


Figure 1.4 Pulsed I-V measurement waveform shape and sampling time window representation.

The trapping of charge carriers is known to affect III-V devices, namely high power GaN HEMTs. This occurs at time-scales which are below the high-frequency charge storing phenomena, ns, and above thermal effects, ms. Therefore, with a high peak power pulsed I-V measurement system, able to provide voltage and current pulses or other pulse-shaped waveforms at the µs scale, these phenomena can be observed, and characterized.

1.5 Dissertation Objectives

The purpose of the work here reported was to develop and implement a pulsed I-V measurement setup in order to observe and characterize LTME caused by the trapping of charge carriers in RF power GaN HEMTs. To accomplish that goal, and given that dedicated pulsed measurements hardware are extremely costly and their flexibility is somewhat limited, an "in-house" measurement setup was developed, relying on two electronic circuits that were designed and implemented, called throughout this document as pulsers. The setup was controlled through MATLAB scripts such that pulsed I-V curves could be obtained with some flexibility in the pulse widths, periods and shapes used. Through properly designed pulsed excitations, LTME could be observed in the measured I-V curves and their time constants extracted.

1.6 Dissertation Outline

This document is organized as follows.

Chapter 2 overviews the most common RF power transistors modelling techniques, with emphasis on compact models. Additionally, the extraction of a bias-dependent small-signal equivalent circuit from pulsed S-parameters is described.

Chapter 3 presents the development of a pulsed I-V measurement setup, including the design of the drain and gate pulsers, as well as the measurement setup block architecture and control methods.

Chapter 4 addresses LTME, in particular those related to charge carriers trapping phenomena and how pulsed DC I-V measurements can be used to characterize and model these effects.

In Chapter 5, the conclusion as well as further work steps are provided.

Chapter 2

RF Power Transistors Modelling

During circuit and system design process, CAD software is an essential tool, in both industry and research. It is, therefore, fundamental to provide RF circuit designers with accurate and reliable models that can help reducing time and production costs. These better models may, ultimately, lead to first-pass designs instead of the time-consuming iterative design processes. Transistor models should be easily extractable and to include in commercial simulator software. Convergence and simulation speed are also important features researchers and designers usually take into account.

There are mainly three types of modelling approaches: physics based, compact and behavioural modelling. Models based on the physical structure of the device are fundamental when developing new materials and technologies. They can be very insightful and cover wide device operating ranges but the complexity in their extraction and the processing time required to solve the associated complex difference equations in simulators, such as Poisson's and the electron and hole continuity equations are major drawbacks, even in a powerful computer. Furthermore, they are less flexible, since a new device structure or material may require a very different model.

Compact models, are half-way between the physics approach and a completely empirical one. They still rely on the nature of the device but reduce much of the physics computation complexity making use of equivalent circuit elements and a set of parameters which are intended to be easily extractable.

Behavioural, black-box or measurement based, models map the input output relationships with none or very few previous knowledge about the device or system to be modelled. These are more often used at a higher level of abstraction in overall circuit and system design [13].

Compact models may also be divided into physics-based or measurements based. The former make use of the physical properties of the device such as its structure dimensions and doping level [14], whereas in the latter, semi-empirical parameters or a set of look-up table (LUT) are extracted from device measurements, both containing one or more linear or non-linear equivalent circuits. The behavioural model approach resembles the measurement based compact model despite being defined separately, due to the more mathematical and systematic nature. Figure 2.1 shows a general comparison between different modelling approaches.

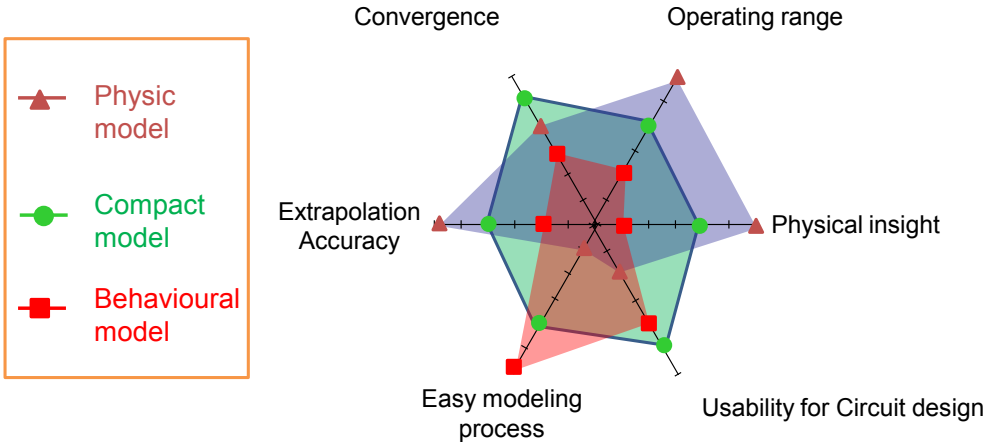


Figure 2.1 Qualitative comparison between different RF PA modelling approaches, adapted from [15].

Compact models are very often used by circuit designers and regarded as the industry standard. This modelling approach will be the one used in this work. Table 2.1 contains some FET and HEMT commercial available models.

FET Model	Number of Parameters	Thermal Effects	Trapping Effects	Original Device Context
Curtice3	59	No	No	GaAs FET
CFET	53	Yes	No	HEMT
EHMET1	71	No	No	HEMT
Angelov	80	Yes	No	HEMT/MESFET
AMCAD HMET1	65	Yes	No	GaN HEMT

Table 2.1 Common commercial models for GaN HEMTs, adapted from [16].

The compact model parameter extraction is a fairly difficult and time-consuming process. A generic model extraction flow, Table 1.1, involves different measurement procedures. The two most important are pulsed I-V and pulsed S-parameters. With these measurements the core device model can be created as a LUT, indexed by the terminal voltages, v_{GS} and v_{DS}. This can thus be regarded as a non-linear model made of a set of liner-models although care should be taken on how the data is interpolated between sets. The LUT approach may result in large amounts of data and usually a suitable non-linear analytic model, whose parameters can be fitted to the measurement data, is used. This model is then called a non-linear compact model as it is much lighter than the LUT approach, given that only a set of parameters need to be stored. The current-source and some capacitances are typically modelled as non-linear while other equivalent circuit elements are standard linear components commonly used in simulators.

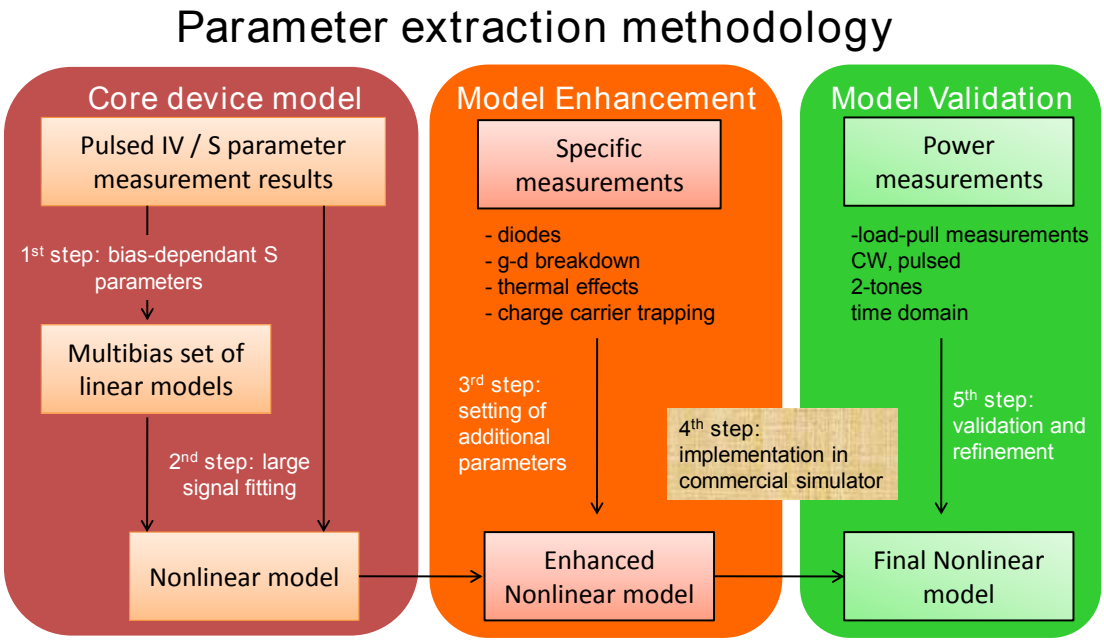


Figure 2.2 Modelling procedure flowchart, reprinted from [17].

After the core model is extracted, extra features can be added to it. Less important characteristics such as parasitic junction diodes and breakdown may also be added. Thermal effects and charge carrier trapping are, however, very important features that can change dramatically the device model behaviour affecting its operation in a PA circuit. Therefore, modelling both trapping and temperature effects is of paramount importance for accurate simulation results.

When the complete model is extracted, many types of validation and performance measurements can be taken and their results used for further refinement of the model. Usually, PA designers want to achieve the highest possible efficiency and output power while keeping sufficiently high linearity. That is why most models are designed and extracted to predict, as accurately as possible, the figures of merit related with these requirements, such as IMD, power-added efficiency (PAE), etc.

During the development of the transistor model, we should bear in mind the following Laws of Simulation and Modelling [13]:
(i) A simulation is only as accurate as the models it is based on;
(ii) A model is (mostly) useless unless it is embedded in a simulator;
(iii) Models are, by definition, inaccurate; it's just a matter of degree;
(iv) Models generally trade off complexity (simulation time) for accuracy.

2.1 DC Modelling: I-V Curves

The DC behaviour of a FET, or other types of transistors, is usually expressed trough an I-V plot. This type of representation is very compact since just one graph may contain much information about the behaviour of the transistor. I-V graphs drawn from the same transistor can change dramatically according to their measurement conditions. That said, it is very important to mention under which measurement conditions the data used in these graphs was obtained. The x-axis represents V_{DS} and the y-axis I_{DS}. Usually, several curves are drawn, one for each gate voltage, V_{GS}.

Figure 2.3 shows a typical I_{DS}-V_{DS} plot of a FET. Several effects are emphasized on the curves, particularly the drain current decrease due to thermal effects. This characteristic appears when the I-V curves are based on DC measurements and the power dissipated at device, i.e., the $I_{DS} \times V_{DS}$ product, is sufficiently high to induce self-heating and cause a current decrease. Note that, if the curves in Figure 2.3 represented the actual dynamic behaviour under RF operation of the transistor, a strange phenomena would appear to happen, given that the negative slope of the curves measured at higher V_{ds} would mean a negative drain resistance, R_{ds} , or conductance, g_{ds}.

DC I-V measurements are simple, fast and widely used, mostly for small gate-periphery devices, i.e., low power devices requiring small amounts of current. This type of measurements is extremely important since the main non-linearities of a FET come from its voltage-current relationship and so these constitute an important starting point for the large-signal

model [13]. To be able to produce I-V plots which are not temperature dependent, pulsed I-V measurements were introduced. This type of characterization is one of the topics of this work and will be addressed in Chapter 4.

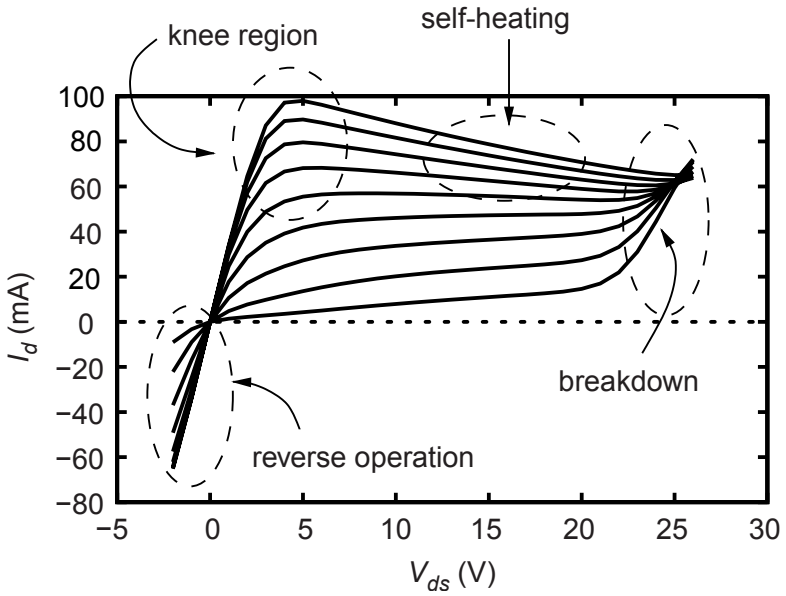


Figure 2.3 Typical DC I-V curves of a FET highlighting different typical characteristics of these devices, reprinted from [18].

2.2 Small-Signal Equivalent Circuit: SSEC

S-parameters are the most used measurements in order to capture the RF behaviour of a device under test (DUT). Being a linear representation of the high frequency behaviour of the device, they accurately represent its operation in the small signal regime at the operating bias point, V_{DS_q} and I_{DS_q}, under which they were measured. Therefore, a set of S-parameters must be taken for each different bias so that one can get the device RF behaviour at all the regions of interest.

Having in mind the way S-parameters measurements are taken for each bias condition of a FET, one can better understand the meaning of the small-signal equivalent circuit (SSEC). That is also one of the reasons for the compact model naming, since the physical phenomena of a rather complex device is mapped through an equivalent circuit. Although most of the extracted elements are indeed well described as linear, some of them are converted to non-linear, either through the use of properly fitted mathematical functions or by using LUTs

indexed by the terminal voltages at the device. The former can model accurately the extracted parameters and be continuous and differentiable up to a given order, depending on the quality of the mathematical functions used. The latter are a direct result of the circuit parameters extracted from the S-parameter data which need to be interpolated or processed in order to cover the device's full operating range and be useful for non-linear simulations.

To obtain the SSEC model a sequential procedure is used to extract the circuit elements. As pointed in [16], one of the SSEC advantages is that it links the physical structure of the device to its circuit behaviour allowing the connection between the RF performance and the geometry of the device. It is also important to notice that models and their associated extraction procedure, which are known to work well for a matured technology such as GaAs metal-semiconductor FET (MESFETs) may provide less reliable results for less mature ones, such as, GaN HEMTs. In any case, the results of applying the modelling techniques already used for GaAs MESFETs on GaN HEMTs appears to result in fairly good models, since most key features are common to both technologies and the SSEC is a general representation that is relatively flexible.

There are, in literature, many works on small-signal modelling approaches. Three of the more widely known are the ones by Dambrine et al. [19], Berroth and Bosch [20] and Rorsman et al. [21]. A SSEC topology for a general FET is presented in Figure 2.4. From it, one can distinguish two types of elements: extrinsic and intrinsic. The structure that surrounds the die, which includes or may include the bond-wires, pre-matching capacitors, the substrate, access pads and the device's package is represented by the extrinsic or parasitic elements, which are, in Figure 2.4, outside the shaded rectangle. Extrinsic elements are considered to be frequency and bias independent. On the other hand, the transistor die is represented by the intrinsic elements which are still modelled as frequency independent but now as bias dependent and are, thus, extracted for each bias point.

The SSEC adopted here, especially the extrinsic part, is a fairly simplified and general one, whose structure is more suitable for smaller devices. When modelling devices of larger gate periphery and/or an higher accuracy is desired, effects like inter-bond-wire capacitances and mutual inductances as well as substrate leakage, can be added to the SSEC. Hence, more extrinsic equivalent circuit elements are needed, which can even be of distributed nature, e.g., transmission lines.

To determine the extrinsic parameters one can choose between two approaches [16]: using dummy structures, i.e., removing the active part of the device and perform measurements with just the remaining passive structure, or applying the 'cold-FET' technique, i.e. measur-

ing S-parameters at $V_{DS} = 0$ V for two different gate conditions: strong forward bias and below pinch-off.

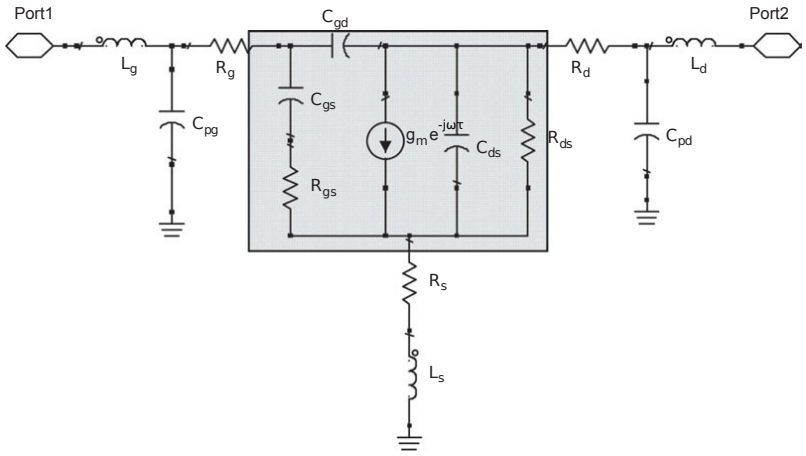


Figure 2.4 Small signal equivalent circuit topology, SSEC, adapted from [18].

The aim of the 'cold-FET' technique is to put the transistor under two different conditions at which the effect of the extrinsic structure will become minimally affected by the active die and, thus, easier to extract. Figure 2.5 shows the inside of two different HEMT packages revealing some of the extrinsic structures previously mentioned.

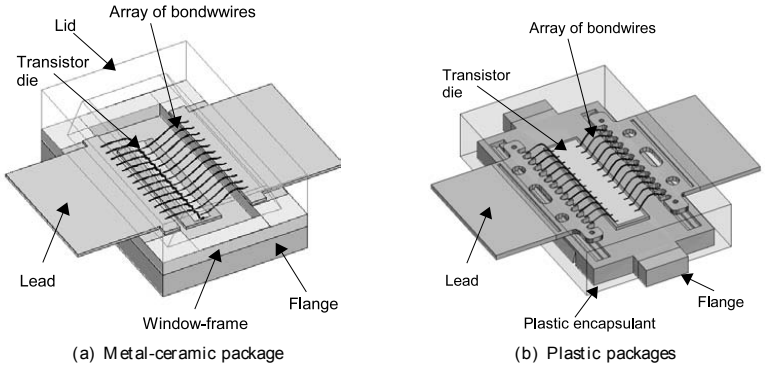


Figure 2.5 RF power transistor plastic and ceramic packaging examples, reprinted from [13].

After determining the extrinsic elements one can proceed to the de-embedding of the intrinsic S-parameter by removing the effect of each extrinsic element from the global S-parameter data. This is done by changing appropriately from S to Z or Y parameters while removing the contribution of this elements from the global S-parameters, as reported in [19]. It is important to refer that errors in the extrinsic parameter extraction and de-embedding will most probably affect the following steps. This will make the model less accurate, either due to the choice of an inadequate model topology, a poor extraction method or even both.

The parasitic inductances are extracted first from the high frequency imaginary part of the Z parameters when the device is biased with $V_{DS} = 0$ V and $V_{GS} = 2$ V. The extracted inductances are then de-embedded from the from the Z-parameters for $V_{DS} = 0$ V and $V_{GS} = -4$ V and these are converted to Y-parameters to find the capacitances. However, the direct application of the method in [19] resulted in negative values for the intrinsic capacitances. Therefore these were set to 0. The extrinsic resistances were determined according to [19] assuming that $R_s \approx 0\ \Omega$. This provided physically consistent results, i.e., the resulting S_{11} and S_{22} after de-embedding, stayed inside of the Smith Chart. The parameters extracted from pulsed S-parameter measurements (obtained through an Auriga system) of a 3.3 W, 1 mm gate periphery GaN HEMT from *SEDI, Inc.* biased at $V_{ds,q} = 50$ V and $V_{gs,q} = -5$ V are shown in Table 2.2. Despite having set to 0 the parameters that could not be extracted, all the remaining ones provided a reasonably good starting point suitable for further refinement through optimization in a CAD software tool after a first guess for the complete model, including the intrinsics, is determined.

Parameter	**Value**
L_d	85.4 pH
L_g	50.4 pH
L_s	5.2 pH
R_d	3.85 Ω
R_g	0.97 Ω
R_s	0 Ω
C_{pd}	0 pF
C_{pg}	0 pF

Table 2.2 Extracted extrinsic parameters for a 3.3 W GaN HEMT.

The intrinsic part of the SSEC, inside the rectangle in Figure 3.4, is often represented using Y parameters. These are better suited to describe the π-topology of the SSEC and result in simpler expressions for estimating the element values at low frequencies. Without the extrinsic elements, the SSEC can be expressed as follows,

$$Y_{int} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} Y_{gs} + Y_{gd} & -Y_{gd} \\ -Y_{gd} + \dfrac{g_m e^{-j\omega\tau}}{1 + j\omega R_{gs} C_{gs}} & Y_{ds} + Y_{gd} \end{bmatrix}, \tag{2.1}$$

with,

$$Y_{gs} = \frac{1}{j\omega C_{gs}} + R_{gs}, \quad (2.2) \qquad Y_{ds} = \frac{1}{R_{ds}} + j\omega C_{ds}, \quad (2.3) \qquad Y_{gd} = j\omega C_{gd}, \quad (2.4)$$

and each parameter can be estimated through the following relations,

$$C_{gd} = -\frac{1}{\omega} Im\{Y_{12}\}, \quad (2.5)$$

$$C_{ds} = \frac{1}{\omega} Im\{Y_{12} + Y_{22}\}, \quad (2.6) \qquad R_{ds} = Re\{Y_{12} + Y_{22}\}^{-1}, \quad (2.7)$$

$$C_{gs} = \frac{1}{\omega} Im\{Y_{11} + Y_{12}\}, \quad (2.8) \qquad R_{gs} = \frac{1}{\omega^2 C_{gd}^2} Re\{Y_{11} + Y_{12}\}, \quad (2.9)$$

$$g_m = |Y_{21} - Y_{12}|, \quad (2.10) \qquad \tau = -\frac{1}{\omega} phase\{Y_{21} - Y_{12}\}. \quad (2.11)$$

Note that in order to separate real and imaginary parts of the Y parameters, a denominator of the type:

$$D = 1 + \omega^2 R^2 C^2, \quad (2.12)$$

appears, and the Equations (2.5) and (2.11) rely on approximations of the same kind as,

$$D = 1 + \omega^2 R^2 C^2 \approx 1, \quad (2.13)$$

which can be made with minimal effect on the final result if the parameters are extracted at low enough frequencies. There is no R_{gd} in series with C_{gd} in Figure 2.4 due to the difficulty in finding a resistive component consistently in S_{12} and S_{21}. Despite that shortcoming, the impact of that element in the circuit behaviour is hardly noticed and some published SSECs do not even consider this element. From Equations (2.5) and (2.11), the intrinsic elements were determined for each bias point, through a linear fit at lower frequencies. The parameter values obtained for $V_{DS} =$ 15 V and $V_{GS} =$ −2.3 V are shown in Table 2.3.

The procedure described before is a generalized one since the extrinsic structure of RF power transistors can be much more complex and also because the method applied was developed for the more mature GaAs MESFET technology. Thus, although it works reasonably well, care should be taken when applying it to GaN HEMTs, especially for the extrinsic param-

eter extraction. In [18], for example, it is referred that the equivalent circuit which represents the transistor in the 'cold-FET' condition will not be easily extractable under strong forward-bias, since the conduction band of GaN HEMTs is much higher than that of GaAs devices.

Parameter	Value
C_{gs}	1.96 pF
C_{gd}	81.93 fF
C_{ds}	0.26 pF
R_{gs}	0.58 Ω
R_{gd}	0 Ω
R_{ds}	590 Ω
g_m	125 mS
τ	5.13 ps

Table 2.3 Extracted intrinsic parameters at $V_{DS} = 15$ V and $V_{GS} = -2.3$ V for the 3.3 W GaN HEMT.

Some of the parameters obtained are depicted in Figure 2.6 versus frequency. The capacitances, g_m and τ remain relatively constant up to 10 GHz and R_{gs} from 2 GHz to 10 GHz.

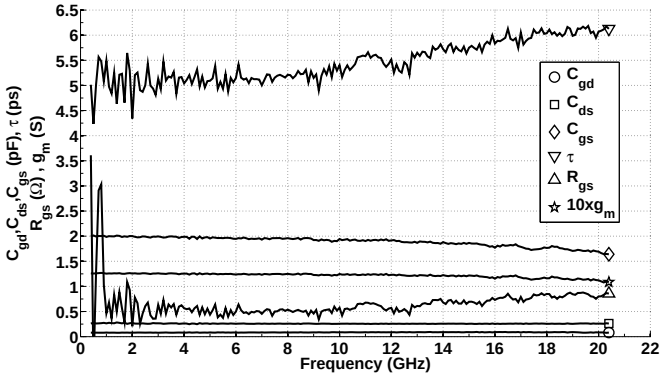


Figure 2.6 Intrinsic parameters versus frequency obtained at $V_{DS} = 15$V and $V_{GS} = -2.3$ V for a 3.3 W GaN HEMT.

This indicates that one has to carefully select which zones to use for the fitting and verify the validity of that choice. It may also be related with the measurement noise which, indirectly impacts the extraction and the parameter equations themselves, as these, are lower frequency approximations taken from an equivalent circuit, itself already an approximation. Nevertheless, the results can be very accurate, actually as accurate as the complexity of the model and the measurements used to build it allow.

2.3 Extending the Model to Large-Signal

The SSEC determined previously is the result of a set of small-signal S-parameter measurements. However, RF power transistors are typically operated under large signals in such a way that the highest possible output power can be drawn from the device with the highest possible efficiency and linearity. Therefore, effects like temperature, junction diodes' behaviour and breakdown should be added to the model. Furthermore, under actual telecommunication signals other important effects, such as long-term memory effects, may degrade the expected performance and, thus, need to be taken into account in a complete model. The capability of the extracted set of small-signal models in predicting distortion in a simulator is limited by the discrete nature of the measurements, i.e., finite amount of data points. Additionally, part of the extracted SSEC parameters are bias-dependent and may result in large amounts of data that need to be stored, which is less suitable to be used in a compact model.

2.3.1 Multi-Bias Linear Models

Although not suitable to include in commercial models, the bias-dependent SSEC data set may be used to validate the extracted model by comparing it with the device S-parameter measurement data. To do so, a model that accesses a LUT was created in Agilent Advanced Design System (ADS), Figure 2.7.

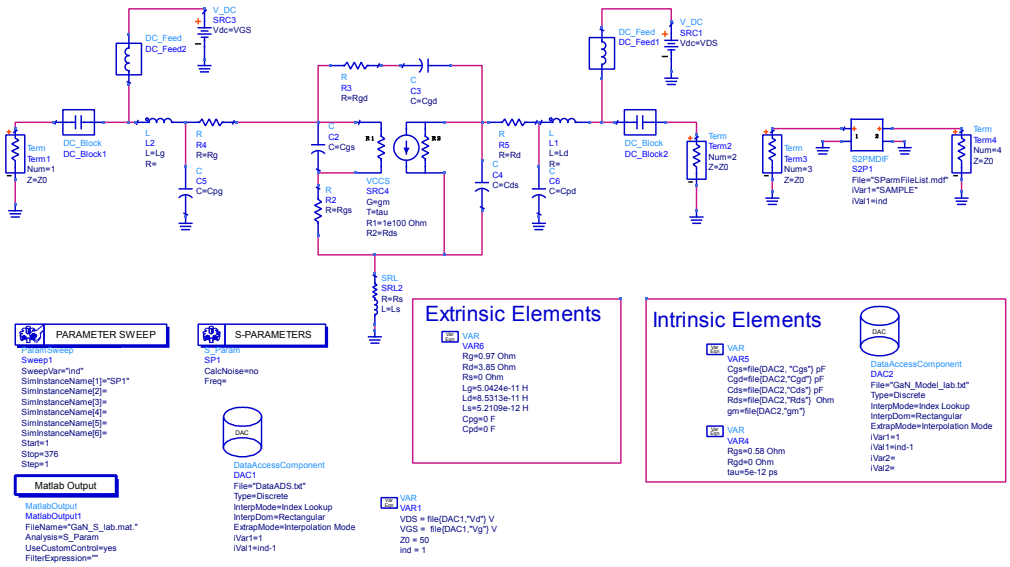
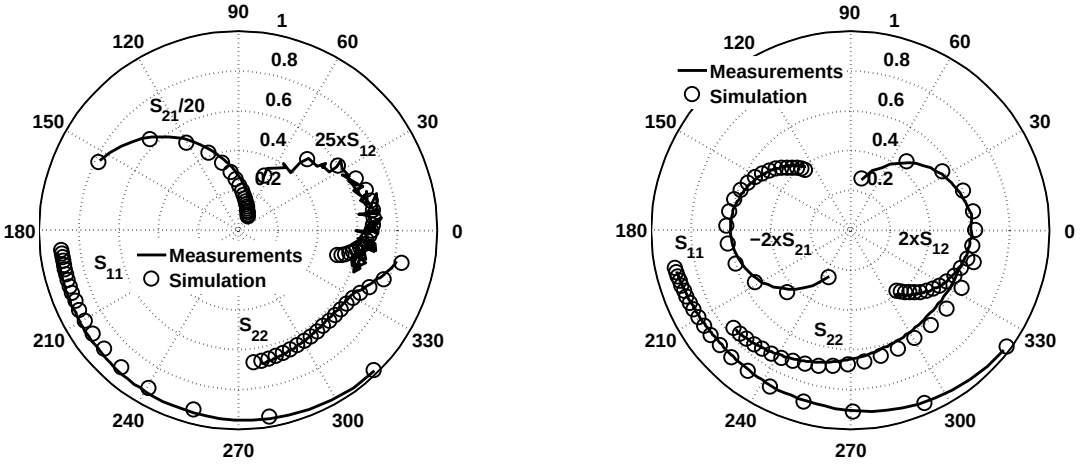


Figure 2.7 SSEC ADS schematic used for comparison with S-parameter measurement data of a 3.3 W GaN HEMT.

The bias-dependent small signal elements were imported from a previously generated file in MATLAB making the overall model consisting of many linear models. The model simulation S-parameter data was exported to MATLAB for comparison with the measured device S-parameters that were initially used to extract the SSEC model.

Figure 2.8 shows the comparison between the measured S-parameter and the simulation of the developed model for two different bias conditions.



(a) $V_{DS} = 30\,\text{V}$ and $V_{GS} = -2.3\,\text{V}$. **(b)** $V_{DS} = 0\,\text{V}$ and $V_{GS} = -2.3\,\text{V}$.

Figure 2.8 Comparison between model and measurements from 500 MHz to 10 GHz.

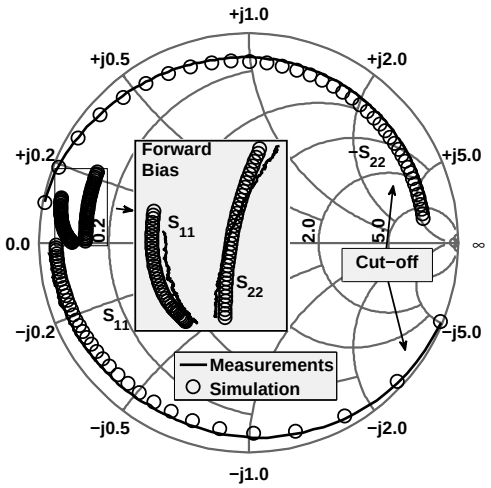


Figure 2.9 Comparison between model and measurements from 500 MHz to 10 GHz under the 'cold-FET' condition ($V_{DS} = 0\,\text{V}$), at $V_{GS} = -4\,\text{V}$ (cut-off) and $V_{GS} = 2\,\text{V}$ (forward bias).

A good match was obtained for a wide range of V_{DS} and V_{GS} voltages. Scaling factors were

used such that S_{12} and S_{21} could be drawn on the same chart. The Smith chart depicted in Figure 2.9 shows the comparison between measured and modelled S-parameters, S_{11} and S_{22}, with the device in the 'cold-FET' condition.

The extrinsic elements were extracted from measurements under the conditions previously mentioned. An inductive behaviour can be observed for strong-forward bias whereas the capacitive nature of the device for the below pinch-off biasing becomes clearly visible. The results from the model simulation are in good agreement with the measurements in this condition too. Note that the cut-off S_{22} in Figure 2.9 is rotated 180° for better visualization.

2.3.2 Non-linear Models

To improve the model compactness and avoid the shortcomings in terms of resolution and lack of continuous differentiability of the LUTs approach, models usually consist of non-linear analytical functions that were fitted to the device's measurement data along V_{GS}, V_{DS} or both. These non-linear functions contain parameters that may be firstly set from visual inspection of the DC I-V characteristics or its partial derivatives, g_m and g_{ds}, extracted from S-parameters of the device and later optimized in a software tool. Depending on the number of parameters and the choice of suitable analytical functions, very accurate and compact models can be developed. Figures 2.10 and 2.11 show two of the non-linear elements extracted from the de-embedded S-parameters, g_m and C_{gs}, which can be fitted to properly selected non-linear functions. It is most noticeable that both parameters are strongly V_{GS} dependent, although some variation with V_{DS} is also visible.

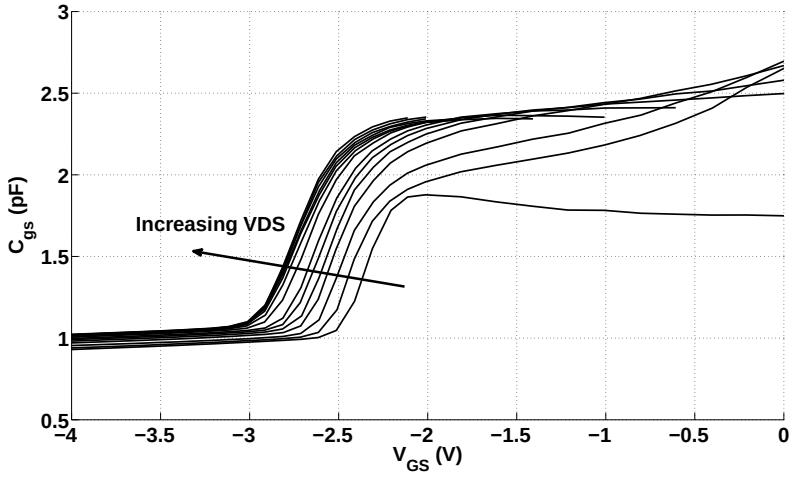


Figure 2.10 SSEC extracted C_{gs} versus V_{GS} for $V_{DS} = 0$ V to $V_{DS} = 100$ V.

After verifying that the extracted parameters are reasonably accurate, one can evaluate how each of the parameters expected to be non-linear varies with gate and drain voltages. If the parameter or equivalent circuit element is strongly dependent on just one input voltage, v_{DS} or v_{GS}, a two-dimensional fitting, in $\mathbb{R}^2$, may be discarded. This will reduce the complexity and avoid non-physical results like violations of the charge conservation principle which may appear when non-linear capacitances are not exclusively dependent on their terminal voltages. Furthermore, the used non-linear mathematical functions are time independent which is referred in literature as the quasi-static approximation [22].

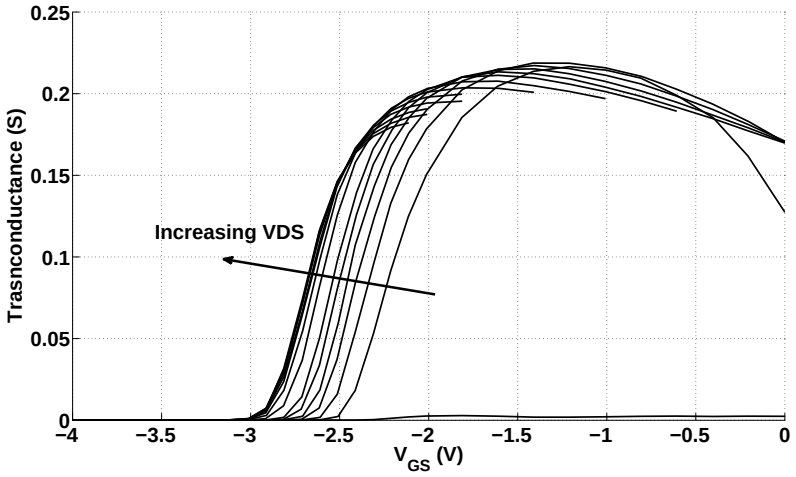


Figure 2.11 Extracted SSEC g_m versus V_{GS} for $V_{DS} = 0\,\text{V}$ to $V_{DS} = 100\,\text{V}$.

The author of [23] describes a non-linear current source model used for a GaN HEMT. That model will be the used in Chapter 4, with the addition of a charge carrier trapping related LTME part, obtained from pulsed DC I-V measurements. Similarly to other models proposed in literature, it can be generally expressed as,

$$i_{DS}(v_{GS},\, v_{DS}) = \beta \cdot f_g(v_{GS},\, v_{DS}) \cdot f_d(v_{GS},\, v_{DS}), \tag{2.14}$$

where the output current i_{DS} is defined as the product of two functions, $f_g(.)$ and $f_d(.)$, and a scaling factor, β. Although both drain and gate voltages are input parameters for both functions they are separated and written with different subscripts to represent their stronger relationship with each control voltage. The device threshold voltage is taken into account through the linear function,

$$v_{GS,1}(v_{GS},\, v_{DS}) = v_{GS} - V_T, \tag{2.15}$$

and is usually extracted from the transconductance derivative, g_{m2} peak or second derivative, g_{m3}, null given the soft turn-on nature of the transistor. The gate voltage at which the device starts to enter the saturation region and the smoothness of this transition are controlled by

$$v_{GS,2}(v_{GS}) = v_{GS,1} - \frac{1}{2} \cdot \left(v_{GS,1} + \sqrt{(v_{GS,1} - V_K)^2 + \Delta^2} - \sqrt{{V_K}^2 + \Delta^2} \right), \tag{2.16}$$

which enables the model to replicate the HEMTs typical transconductance decrease. The V_K parameter is just a displacement in effective gate voltage while the Δ controls the smoothness. Given the soft turn-on nature of the device and the need for a consistent definition of V_T, the turn-on itself and its abruptness are defined by,

$$v_{GS,3}(v_{GS}) = V_{ST} \cdot ln \left(1 + e^{\left(\frac{v_{GS,2}}{V_{ST}} \right)} \right), \tag{2.17}$$

meaning that for v_{GS} below V_{ST} the effective gate voltage will tend to zero, whereas, above V_{ST} it will tend to the input itself, v_{GS}.

With all the shaping functions for the effective gate voltage, the complete current source model is built as,

$$i_{DS,1}(v_{GS}) = \beta \cdot \frac{{v_{GS,3}}^2}{1 + \frac{{v_{GS,3}}^{plin}}{V_L}} \tag{2.18}$$

where $plin$ defines the transition between quadratic and linear regions for v_{GS} higher than V_L, which adds the quadratic to linear transition of the $i_{DS}(v_{VGS})$ and introduces the transconductance gain, β. The non-null drain conductance, g_{ds}, is included through a linear factor,

$$i_{DS,2}(v_{DS}) = (1 + \lambda \cdot v_{DS}) \tag{2.19}$$

and an hyperbolic tangent is used to model the transition between triode region and saturation and the displacement of the knee voltage with v_{GS},

$$i_{DS,3}(v_{GS},\ v_{DS}) = tanh \left(\frac{\alpha \cdot v_{DS}}{{v_{GS,3}}^{psat}} \right). \tag{2.20}$$

with $psat$ setting the dependence on v_{GS} of the triode to saturation region transition, resulting in,

$$i_{DS}(v_{GS},\ v_{DS}) = i_{DS,1}(v_{GS}) \cdot i_{DS,2}(v_{DS}) \cdot i_{DS,3}(v_{GS},\ v_{DS}). \tag{2.21}$$

It is also known that the threshold voltage, V_T, varies with v_{DS} which can be added to the model through

$$V_T(v_{DS}) = V_{T0} + A_{VT} \cdot tanh(K_{VT} \cdot v_{DS}). \tag{2.22}$$

The non-linear model described above can accurately fit the standard I-V characteristics of GaN HEMTs, the gm and gds extracted from small signal S-parameters and also its higher order derivatives, which are of great interest given their impact on the non-linear behaviour of the device.

The intrinsic capacitances, C_{gs}, C_{gd} and C_{ds} may also be modelled with non-linear functions if they significantly vary with gate and/or drain voltages. A typical and versatile empirical formulation is as follows,

$$C(v) = C_0 + \frac{A_C}{2} \cdot (1 + tanh[K_C \cdot (v - V_C)]), \tag{2.23}$$

where V_C and K_C control the transition voltage and its abruptness from the initial C_0 to C_0 + A_C. This formulation is most suitable to model C_{gs} depletion capacitance but may also work reasonably well for C_{ds} and C_{gd}. Note that, physically, these capacitances may depend on both v_{GS} and v_{DS} but the complexity of a fit in the $\mathbb{R}^2$ space is usually not worth the accuracy improvement it brings to the model.

2.4 Model Enhancements

The model described so far focused on the current source and non-linear capacitances only. Hence, several secondary and often undesirable effects shall be included in order to increase the model accuracy and operating range. PAs are not able to reach 100 % efficiency, which means that they will be dissipating some amount of power depending on their total output power and efficiency. This power will heat up the device and greatly affect its I-V characteristics. Furthermore, the heating and cooling processes have associated long time constants, which also lead to long-term memory effects. Other characteristics only noticeable under extreme operating conditions may be included such as forward bias of gate-source junctions and drain-source breakdown. A very important source of long-term memory effects is the trapping of charge carriers in the device, particularly in III-V technologies, where GaN HEMTs are included, the observation and characterization of these effects on a real device will be further discussed in Chapter 4.

2.4.1 Thermal Effects

Due to the non-finite thermal conductivity of materials, the heat generated in channel of an RF transistor when it is under RF operation or just biased with DC voltages will increase the temperature above the one of the substrate. This increase can be simply formulated as,

$$T_{dev} = T_{sub} + R_{th} \times P_{diss} = T_{sub} + R_{th} \times (I_{ds} \times V_{ds}), \tag{2.24}$$

where T_{dev} is the device's average temperature. Since power transistor are typically fabricated with multiple smaller cells in parallel to achieve higher currents and, thus, higher output powers.

The thermal impedance may be extracted from 3D thermal simulations or carefully designed temperature related measurements, relying on thermally controlled chucks or on infrared (IR) thermometers when the device is not packaged. The temperature rise and fall can have very long time constants and its effect on the device's I-V curves is highly noticeable in a decrease on the I_{ds} current when the temperature in the device increases. Figure 2.12 shows the effect that temperature has on the I-V curves of a pseudomorphic HEMT (pHEMT). The decrease in current reaches more than 20 % at the higher V_{gs} curves.

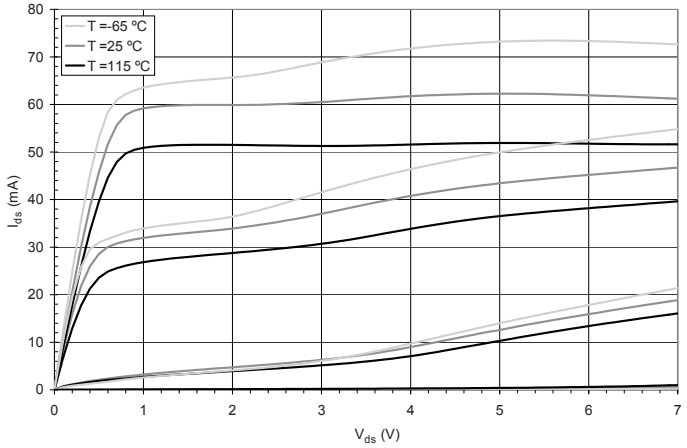


Figure 2.12 Temperature effect on a pHEMT, reprinted from [18].

A practical approach is to include all the device temperature effects in the non-linear drain current model, $i_{DS}(v_{GS}, v_{DS}, f(T))$, previously developed for the isothermal model. An equivalent R-C network, depicted in Figure 2.13, is often used to model temperature effects. The power generated in the device is included as a current source, while the circuit voltages represent the temperatures. A voltage source is used to set the reference temperature. The simu-

lated temperature is then used as the input of the scaling function applied to the drain current model.

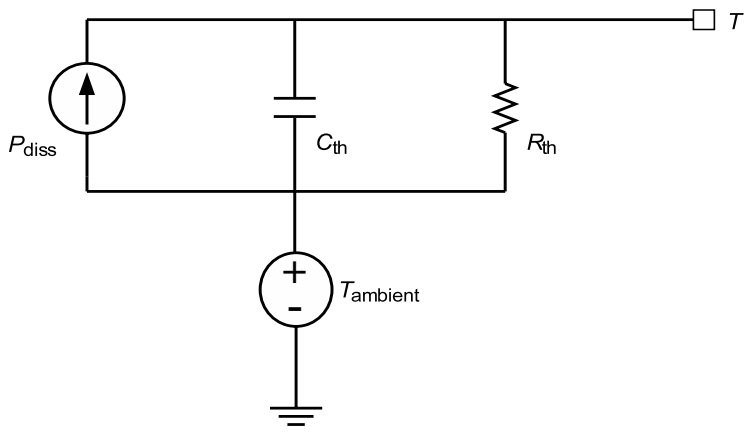


Figure 2.13 Thermal RC sub-network of the equivalent-circuit thermal model used to calculate current degradation from average dissipated power, reprinted from [13].

The usage of R-C networks make the differential equations associated with heat flow and temperature self consistent and, thus, easier to solve in circuit simulators. These dynamically couple the thermal and electrical physics of the device, which is of great importance in a full electro-thermal model. Compact models usually include other temperature related effects, such as the extrinsic resistance and bond-wires temperature dependence in the drain current, i_{DS}, model function. This is more convenient because extrinsic elements can still be modelled as linear.

2.4.2 Gate-Source Diode

The gate source junction diode of III-V HEMTs is formed by a metal-semiconductor contact and can be approximately modelled as a Schottky junction, using the Shockley diode formula:

$$i_G(v_{GS}) = I_s \cdot \left(e^{\left(\frac{v_{GS}}{\eta \cdot V_T}\right)} - 1 \right), \tag{2.25}$$

where I_s is the reverse saturation current and V_T is the thermal voltage, which is approximately 25 mV at room temperature, given by,

$$V_T = \frac{kT}{e}, \tag{2.26}$$

with e the electron charge , k the Boltzman's constant and T the absolute temperature in Kelvin. The actual FET may have many hetero-junction diodes from gate to source or gate to drain, but since the gate-source junction is typically heavily reverse biased and may become forward biased only for some part of the RF period, modelling it with a fitted exponential provides reasonable accuracy.

2.4.3 Voltage Breakdown Modelling

Breakdown voltage is a very important specification of an RF power transistor. It is a major constraint on the maximum output power at which the device can operate. The breakdown voltage is often defined as the maximum v_{DS} a transistor can safely withstand without breaking down its channel near the drain.

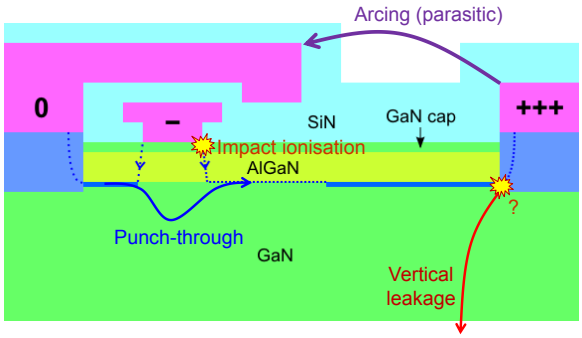


Figure 2.14 Breakdown mechanisms in a general GaN HEMT, reprinted from [11].

This often irreversible phenomenon has several origins, either extrinsic, like air ionization or intrinsic, Figure 2.14. Within the latter, the most common are impact ionization and consequent avalanche breakdown caused by the high fields generated between the drain and gate electrodes. This will cause an exponential increase in the drain current and temperature such that the device can ultimately burn-out. There are, however, other high-voltage breakdown mechanisms but these are less critical to the normal operation of the device in a PA.

Some fabrication techniques may increase the breakdown voltage. One of those techniques is the addition of one or more electrodes between the drain and gate terminals, connected to the gate or to source(ground), called field-plates. These plates act similarly to a Faraday shield blocking high electric fields. Pulsed measurements are a good way to probe the breakdown regions and characterize the device behaviour in those regions, such that, this behaviour can be included in the model.

One common way of accounting for the voltage breakdown is to use an exponential to model the rapid increase of the drain current. For example, the MET model used for Si LDMOS devices includes the following expression,

$$i_D^{total} = i_{D0}\left(1 + K_1 e^{V_{BReff1}}\right), \tag{2.27}$$

where V_{BReff1} depends on the drain-source voltage and K_1 is a fitting constant [13]. This exponential characteristic exist in GaAs and GaN and can be modelled similarly. i_{D0} is the drain current of the model without the breakdown effect. Modelling these effects is sometimes a challenge given that compact models rely on well behaved functions which are continuous and differentiable. Therefore, adding more exotic effects like breakdown may affect the convergence of the complete model in the circuit simulator.

Chapter 3

Pulsed I-V System Design and Implementation

3.1 Pulsed I-V/RF Systems Overview

The I-V characteristic of a transistor is a compact but very useful representation of its low frequency behaviour. Therefore, to model a FET or HEMT, it is an essential first step to accurately characterize its drain current response to the input voltage stimulus at the gate and drain and plot that as I-V curves. To do so, one can start by simply applying DC voltages at the gate and drain and measure the device's drain current. However, when a constant drain voltage is applied and the generated drain current is also constant, the device temperature may increase due to self-heating caused by the power being dissipated at the device. This temperature change will then be an extra variable one has to take into account because it will affect the device behaviour. In order to mitigate that issue one can perform the so-called pulsed I-V measurements. With that type of characterization, one can observe the behaviour of the FET at areas in the voltage-current plane where DC measurements would damage or destroy the device. These areas are relevant, at least in large signal operation, and so it is important that measurements can also be made there.

The temperature at the device is directly related to its quiescent state and one can pulse its gate and/or drain terminals from that state to any voltage within the safe operating limits. This can be done with minimal changes to the device average temperature if the pulse's period is sufficiently short and long pulse repetition rates are used, i.e. very low duty cycles. Measurements taken under those conditions are said to be isothermal. These measurements are suitable for the electro-thermal modelling of the device since one can characterize it with

several pre-defined temperatures set by its quiescent state and/or any thermal control system. Furthermore, as described in Chapter 2, when using a FET or HEMT in RF PAs, short and long term memory effects will be present. The later can be due to the device itself and/or related to the bias networks. Pulsed I-V measurements are thus very appropriate for observing those long-term memory effects.

3.1.1 Pulsed Measurements

Pulsed measurements provide much insight in terms of thermal and trapping behaviour. By just changing the pulse waveform characteristics, in terms of amplitudes and timings, one can get much insight about the device being characterized [24]. References in literature about semi-conductor devices pulsed characterization are as old as 1967 [25]. However, the first reported pulsed I-V systems date back to the late 1980's and early 1990's [26–29].

3.1.2 Commercial Pulsed Measurements Systems

Complete or modular Pulsed I-V measurement systems have been used for many decades and are offered by specialized companies like Focus Microwaves [30], Maury Microwave [17], Auriga Microwave and Keysight Technologies [31]. Complete solutions resulting from partnerships between those companies are also available. Figure 3.1 shows two examples of pulsed I-V measurements systems. In order to get accurate measurements, one has to reduce parasitic resistances and inductances using the shortest possible cabling. This will mitigate eventual oscillations at the FET or DUT, especially at low frequencies. Good interconnections are important as well, in order to guarantee the best pulse integrity.

Figure 3.1 Commercial pulsed I-V systems. Left: Agilent (now Keysight) Power Device analyser/Cruve Tracer, reprinted from [31]. Right: Maury Microwave/AMCAD Engineering pulse I-V system, reprinted from [17].

The specifications of pulse systems are fairly variable and depend on their target applications. However, it is common to find pulse periods ranging from hundreds of ns to ms available with repetition rates from tens of Hz up to hundreds of kHz. The peak power capability of such systems can reach several kW's. These specifications are interdependent on, for example, the pulse widths, due to design limitations, when very high peak voltages and currents are required, Figure 3.2.

PULSER HEAD SPECIFICATIONS						
SPECIFICATION:	**PHG1001**	**PHD1020**	**PHD1100**	**PHD1300**	**PHD2010**	**PHD2050**
Max Voltage	±20 V	220 V	220 V	220 V	600 V	600 V
Max Current Pulsed	100 mA	2 A	10 A	30 A	1A	5 A
Max Current DC	100 mA	0.85 A	1.7 A	5.0 A	1.0 A	1.0 A
Typical Error	0.1%	0.1%	0.01%	0.01%	0.01%	0.01%
Max Power	2 W	40 W	200 W	1000 W	200 W	1000 W
Min Pulse Width	200 ns	200 ns	750 ns	1000 ns	70 ns	70 ns
Max Pulse Width	See **RF Performance by Pulser Head** plots below					
Max Pulse Repetition Frequency (PRF)	250 KHz @ 20 V	20 KHz @ 200 V 80 KHz @ 100 V	20 KHz @ 200 V 80 KHz @ 100 V	20 KHz @ 200 V 80 KHz @ 100 V	200 KHz @ 200 V	200 KHz @ 200 V
Min Output Rise/Fall	30 ns	30 ns	55 ns	60 ns	35 ns	35 ns
Test Port Connector	BNC (f)	BNC (f)	BNC (f)	BNC (f)	High-voltage BNC (f)	High-voltage BNC (f)

Figure 3.2 Specifications for several pulser heads available from Auriga Microwave, reprinted from [32].

Figure 3.3 shows available pulser heads that can be used without the main system. A complete measurement system can cost several hundred thousand €'s while the pulser heads individual prices can reach tens of thousand €'s.

Figure 3.3 Pulsed I-V header options. Left: Standalone pulser head adaptor from Auriga Microwave, reprinted from [32]. Right: Modular pulsed I-V heads from Focus Microwaves, reprinted from [33].

Typically, pulsed I-V systems consist of a main device, which may have its own internal

power supplies/converters, measurement software and graphical user interface. The main unit synchronizes all the pulse timings and processes the data collected from the pulser heads. Features like de-embedding of parasitic resistances, measurement window definition, averaging and so on may be available depending on the system. There are systems which are modular and allow the usage of the gate and/or drain pulser heads individually. Hence, they need to be integrated in a setup with additional general equipment such as, power supplies and oscilloscopes. This, of course, requires much more effort for proper measurement synchronization and data acquisition and processing.

3.1.3 Pulsed Measurement Systems Reported in Literature

There are several works relying on pulsed I-V systems reported in the literature but almost none that focus specifically on the development of a pulsed I-V system or setup. In fact, many works using pulsed DC I-V and/or pulsed S-parameters use either commercial hardware or software or even both. Moreover, pulsed DC I-V systems are typically embedded in larger systems that also measure pulsed S-parameters. That is of interest to microwave and RF PA designers since their designs are to be used at high frequencies at which distributed effects become important and, hence, the pulsed DC I-V curves are no longer sufficient for transistor modelling purposes. However, pulsed DC systems are still needed to provide the pulsed bias to the DUTs for the bias dependent pulsed S-parameters as well as to help in the characterization and understanding of phenomena that may escape, or be harder to capture only with the pulsed S-parameter measurements.

The authors of [34] cite previous works dating from the 80's and 90's that used pulsed I-V measurements to obtain GaAs device characteristics free of thermal induced dispersion effects. They also state that traditional DC curve tracers were not suitable to characterize the III-V RF devices which are field and temperature sensitive, following previously reported discoveries [35–37]. Thus, pulsed measurements with oscilloscopes and pulse generators had been investigated leading to the development of dedicated pulsed systems. The pulsed I-V system used in [34] consisted of commercial instruments and a Versa Module Europa (VME) eXtensions for Instrumentation (VXI) rack as described in [38]. It contained two arbitrary waveform generators (AWGs), ARB in Figure 3.4, amplifiers for the gate and drain pulse generation, a timing unit and current and voltage digitizers. Current measurements were performed through a Hall effect probe. Dedicated pulsed instruments such as the HP 85120A and network analysers could be integrated with the main system enabling pulsed S-parameters at higher peak powers. The system in [38] provided ± 20 V pulses with 1 A peak current rang-

ing from less than 1 μs to over 10 ms and duty cycles of at least 0.1 %. Its specifications were improved in terms of minimum pulse widths and peak power with the addition of a higher power drain pulser and more sophisticated software [34]. The system was used to determine pulse duration and spacing such that the pulsed S-parameters taken were not only isothermal but also isodynamic.

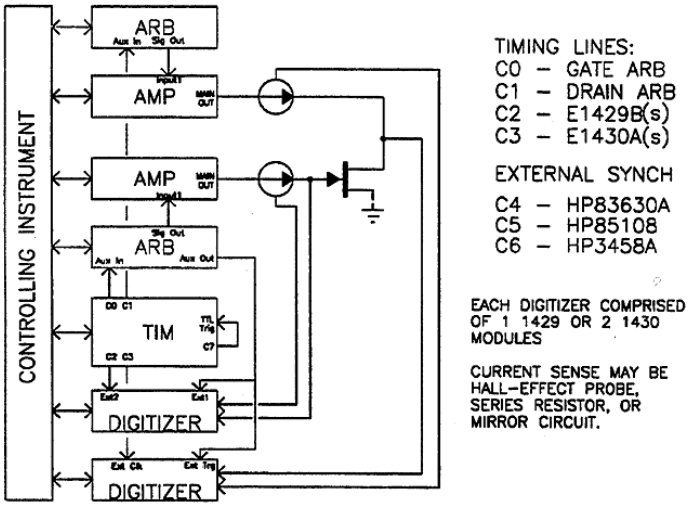


Figure 3.4 Pulsed I-V instrument architecture diagram, reprinted from [38].

The same approach as the one previously described was also taken by the authors of [39]. A VXI rack with a series of commercial devices served as pulsed DC subsystem with a timing controller, two pulsers and two multimeters with a Hall current probe. For the RF subsystem, another commercial instrument was used, an HP 85108A. However, they added an oscilloscope to monitor the pulsed waveforms instead of the digitizers used in the system described previously. That system was able to provide an output peak pulsed voltage of 50 V with quiescent bias DC current up to 600 mA.

The usage of a dedicated pulsed I-V system was reported in [40]. A 386/486 personal computer (PC) with A/D & I/O cards plugged into it, controlled the in-house developed circuitry including a thermocouple and a hot plate for temperature measurement and control. A computer program written in C was developed for the control and automation of the measurements. Its authors also gave some emphasis to the matching of the DUT by using different characteristic impedance cables to connect the DUT to the instrumentation, Figure 3.5. This was done in order to match the different current sensing resistors at the pulse amplifiers output since very narrow pulses, less than 100 ns, were used without including bias-tees in the setup.

In [41], pulsed I-V systems integrated with frequency synthesizers and a spectrum analyser were used to characterize IMD of RF PAs. The main pulsed DC/RF system was automated and controlled by *Agilent's* ICCAP and allowed up to 50 V and 2 A pulses with a minimum width of 1 μs.

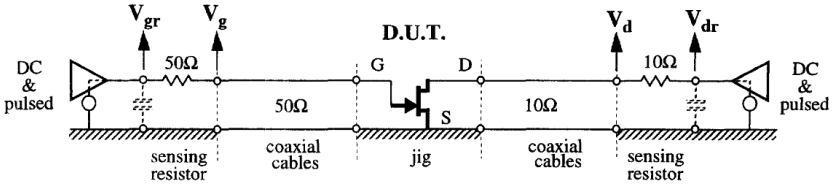


Figure 3.5 Pulsed I-V and the connection between DUT and the instrumentation, reprinted from [40].

A completely new approach, according to its authors, was more recently reported [42]. The new feature in it is the application of the voltage pulses through the bias-tee alternate current AC port contrary to the more standard approach of using the DC port for that purpose, Figure 3.6. This allows a better control of the average voltage and current through the DC port and, since the pulses are generated in the 50 Ω environment, they can be made narrower even with longer cables. In fact, one may think that the DUT is excited with incident pulsed waves instead of pulsed voltages.

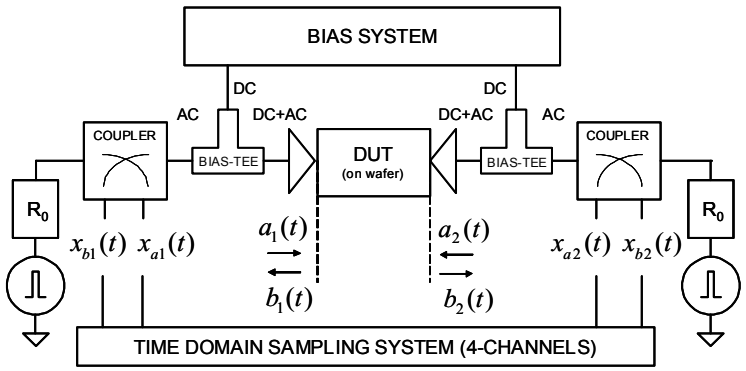


Figure 3.6 Schematic of the new pulsed measurement system, reprinted from [42].

3.1.4 Laboratorial Pulsed I-V System

A very brief review of what is commercially available and what has been published in terms of pulsed I-V measurement systems has been given in the previous paragraphs. As was seen, a pulsed DC I-V measurement system is a crucial tool for the observation and characterization

of LTME of a GaN HEMT. Therefore, an "in-house" laboratorial setup was developed. The followed approach was to use an AWG with an output amplifier/pulser. Thus, except the AWG, the pulsers and the dedicated bias-tees, not more than the general equipment often available at any RF lab was needed:

- DPO3052 digital oscilloscope from *Tektronix*;
  - TCP0030 current probe from *Tektronix*;
  - P6139B 10 MΩ voltage probe from *Tektronix*;
- AWG5012C AWG from *Tektronix*;
- 3 × *TTi* power supplies.

Commercial gate and drain pulsers use two or more internal DC supplies, one for setting the quiescent state and other to provide the pulse voltages, usually through big charge storage capacitors [17]. These devices also have voltage and current measurement capabilities and are able to communicate and send that data to the main control unit. In the developed laboratorial setup, however, an oscilloscope collected the current and voltage waveforms and the excitation pulses were generated by an AWG. The gate and drain pulsers were used to amplify the voltage pulses generated at the AWG and provide enough current to the DUT. Since the AWG output voltage was limited to a couple of volts a good amount of voltage amplification was needed in order to provide high voltage excursions, of up to 50 V. Furthermore, to provide the necessary current to a medium/high power FET or HEMT, the drain pulser was required to have high peak current capabilities.

The measurement system was fully automated through MATLAB software developed for that purpose. The produced scripts managed the measurement process and dealt with the acquisition of data through a general purpose interface bus(GPIB)/local area network (LAN) interface to a PC. Time domain current and voltage waveforms were collected from the digital oscilloscope to the MATLAB environment as well. To obtain the I-V plots, this data needed to be appropriately processed. The design of the pulser circuits and the overall system architecture will be addressed in the following sections.

3.2 Gate Pulser

As mentioned in the previous paragraphs, the developed pulsed I-V measurement setup consisted mostly of general RF lab instruments. However, the pulse waveforms generated by

the AWG are low power signals. Thus, voltage amplification and current buffering was required. The amplifiers designed for that purpose will be referred, from now on, as pulsers, although that designation is more suited to the pulser heads of commercial pulsed measurement systems which include more features than just signal amplification. For the development of the gate pulser a set of requirements were defined:

- Output voltage : −10 V to 0 V;
- Minimum pulse width : 1 µs;
- Capable of driving medium and high power FETs gate ports which can be highly capacitive;
- Adjustable output quiescent voltage.

To meet the aforementioned requirements, an instrumentation amplifier architecture was chosen. It was based on a very fast operational amplifier (OpAmp), a stable voltage reference and an output stage to increase the driving capability of the pulser. Figure 3.7 shows the schematic of the developed gate pulser. The voltage gain was set to be 5 V/V such that a 0 V to 1 V pulse at its input generates 0 V to 5 V pulse at the output and the reference/quiescent voltage was made adjustable through a potentiometer.

The developed gate pulser can also provide output pulses with higher than 0 V amplitudes, up to 10 V, though for GaN HEMTs not more than 1 V can be safely applied at the gate. It consists of three LM7171 OpAmps from *Texas Instruments* that have very high slew rate, 4100 V/µs and a unity-gain bandwidth of 200 MHz. An instrumentation amplifier topology was used because it easily permitted the superposition of the pulse signal with a pre-defined quiescent voltage. The circuit output voltage is defined according to:

$$V_{OUT} = V_{IN} \cdot \frac{R8}{R6}\left(1+2\frac{R4}{R3}\right) - V_{REF} \cdot \frac{R8}{R6}\left(1+2\frac{R4}{R3}\right) \tag{3.1}$$

with $R4 = R5$, $R6 = R7$ and $R8 = R9$. The resistors were chosen so that the overall gain is 5 V/V. The 5 pF capacitors were used to limit the bandwidth of the amplifier, mitigate ringing and prevent oscillations. These capacitors, in parallel with the 2 kΩ resistors, set poles at around 16 MHz reducing the gain at higher frequencies.

The LM7171 has a fairly good current capability, of up to 100 mA. But, since the pulser was intended to be as flexible as possible, and to reduce the OpAmps output currents, an output buffering stage made of bipolar transistors was added to the design. This allows the characterization of higher power devices, that require larger current peaks to charge and discharge

the parasitic and intrinsic capacitances at their gates'. It also permits the application of higher gate voltages to the Device under tests (DUTs), which requires a significant amount of current flowing through the gate of the device. Note that the output stage does not need any biasing as the BJTs are inside the feedback loop of the OpAmp IC4.

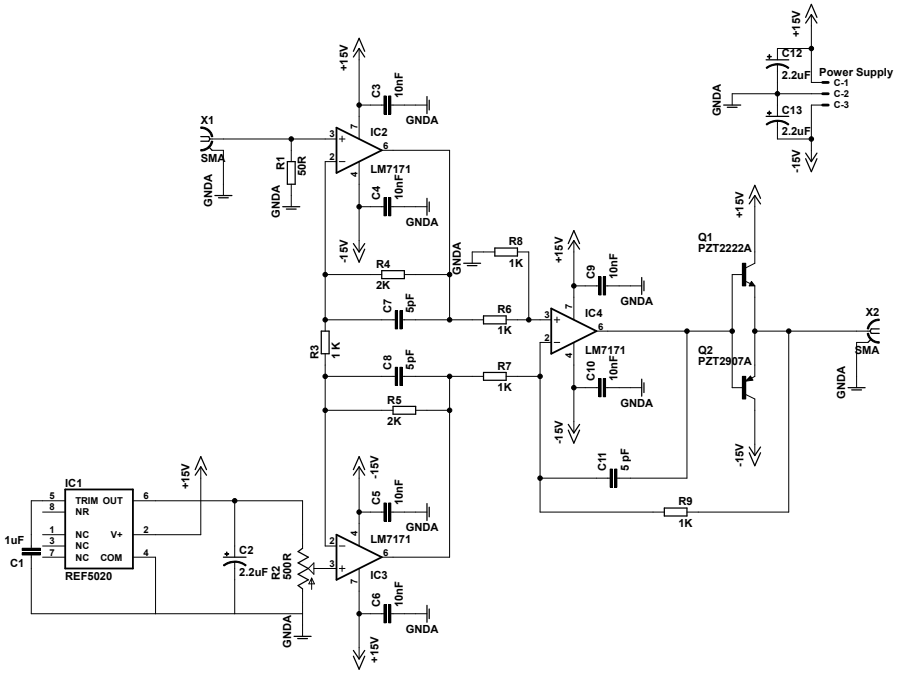


Figure 3.7 Gate pulser circuit schematic.

The gate pulser input, interfaced through an sub-miniature version A (SMA) connector, has a 50 Ω resistor that transforms the high input impedance of the OpAmp non-inverting port into approximately 50 Ω. This matches the AWG output impedance and, thus, avoids signal reflections. The output quiescent voltage is controlled through a multi-turn potentiometer acting as a voltage divider to the 2 V stable reference, REF5020. The use of a stabilized voltage reference is very important for the safe turn on and off of the setup equipment given the *normally-on* nature of GaN HEMT devices. The gate pulser reference voltage was set well below typical HEMT's threshold voltage to prevent unintentional damage to the DUT. When the AWG output is off, i.e., the gate pulser input becomes 0 V due to the 50 Ω resistor to ground, if the manually adjustable reference was not included, the voltage at the FET's gate would be 0 V and any intentional or unintentional drain voltage increase above 0 V could ultimately destroy the device.

Figure 3.8 shows a simulation result of the gate pulser circuit that was built within *Agi-*

lent ADS, Figure A.1 in Appendix A, for a 0.5 µs input voltage pulse. Note that the gate pulser response is well compensated and no overshoot is observed. In fact, the pulser response is actually over-compensated since in this simulation the transistor model used had a relatively low input capacitance. However, it is desirable that, for higher load capacitances, e.g., larger gate periphery devices, the gate pulser response presents minimal ringing. The over-compensation helps achieving that.

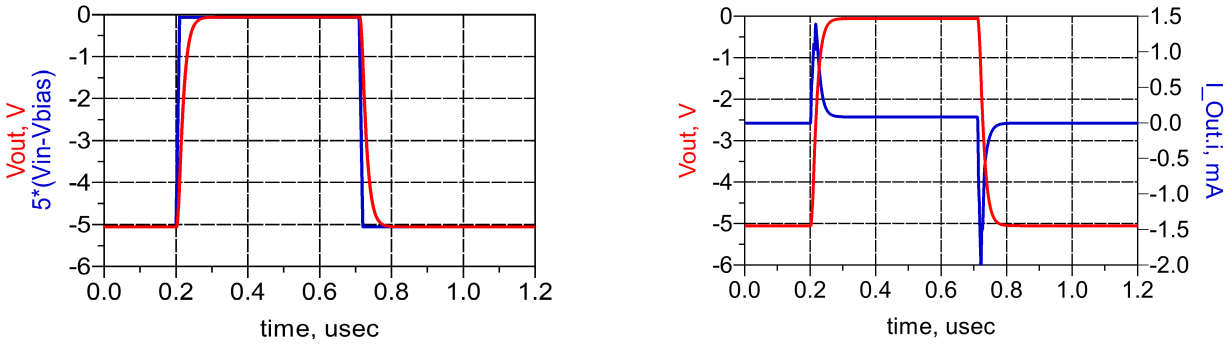
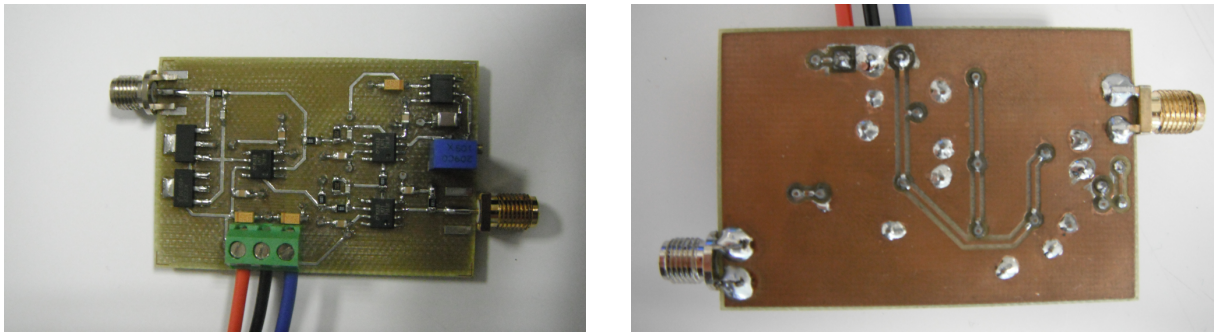


Figure 3.8 Gate pulser simulations with a GaN HEMT model biased at $V_{DS} = 28$ V used as load. Left: input and output voltage pulses. Right: output voltage and current pulses.

The simulated gate pulser was implemented in a printed circuit board (PCB). Figure 3.9 shows the top and bottom view photographs of the designed circuit.



(a) Top-view. **(b)** Bottom-view.

Figure 3.9 Gate pulser PCB implementation.

The signal traces are all on the top plane, whereas the bottom was covered with a ground plane sheet except for some negative voltage supply feeds. Although the pulser was used at very low frequencies, below 10 MHz, an SMA connector was placed at the output to ease the interconnection with the bias-tees used in the measurement setup.

The gate pulser was first tested in two conditions: open output and with a 120 pF capacitor load. The capacitive load emulated the gate of a high power Field-effect transistors (FETs),

although medium power RF devices typically present only a couple tens of pF at their gates. The resulting voltage waveforms are depicted in Figure 3.10.

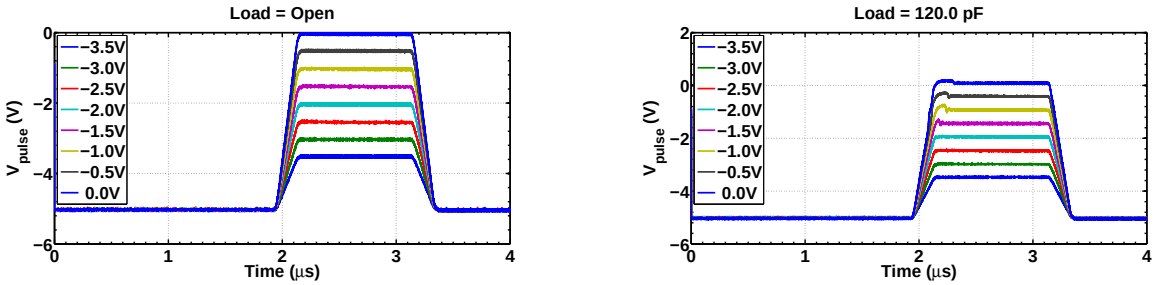


Figure 3.10 Gate pulser response to 1 µs input pulses with 200 ns rise time. Left: No load, i.e., open output. Right: Loaded with a 120 pF capacitor.

Input pulses amplitudes' were first set according to the desired output, knowing the nominal voltage gain of the pulser, 5 V/V. However, the pulser voltage gain may deviate slightly from the nominal value, mainly due to lack of precision in the resistors' values. To overcome that, a calibration factor can be used to calibrate the pulses generated by the AWG accordingly. This factor was determined by the ratio between the measured output pulse voltages applied at the DUT and the desired ones, which were defined during the programming of the AWG. The measured voltages, with gain correction, are in good agreement with the required specifications for the gate pulser, despite the short transient observed for the 120 pF load.

Figure 3.11 shows the output voltages and currents of the gate pulser when driving a *Cree, Inc.*, 15 W GaN HEMT, CGH35015, biased with $V_{DS} = 28$ V.

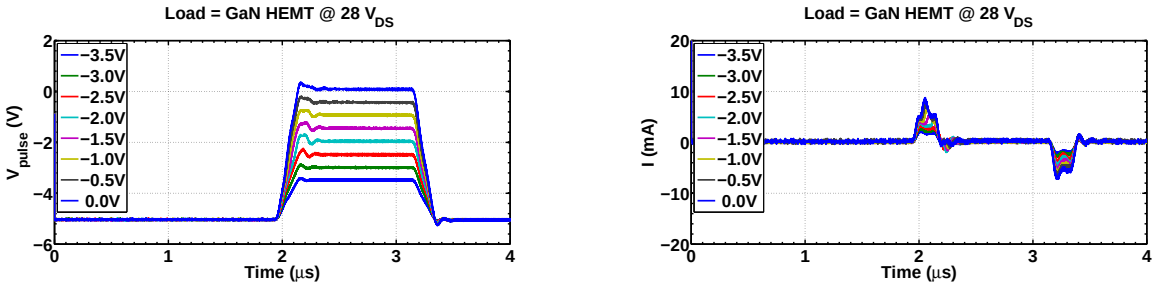


Figure 3.11 Gate pulser response to 1 µs input pulses with 200 ns rise time exciting a 15 W GaN HEMT gate. Left: Output voltage. Right: Output current.

The results follow the previous tests, which already revealed that the required behaviour of the gate pulser was met and that it could be used for the pulsed characterization of GaN HEMTs.

3.3 Drain Pulser

The development of the drain pulser was far more challenging than the gate pulser. Contrary to the gate pulser, the drain pulser requirements in terms of average and peak currents were much more demanding. Additionally, very high voltage gain as well as voltage excursions were required such that the low power pulses from the AWG are amplified and the output can cover the DUT operating voltage range. The drain pulser needs to source the current flowing through the FET or HEMT which can be very high in these RF power devices. Furthermore, it needs to be fast enough to be able to follow the required pulse rise and fall times. The main requirements for the design of the drain pulser were the following:

- Output voltage : 0 V to 50 V;
- Minimum pulse width : 1 μs;
- Capable of providing high peak drain currents, up to 20 A, which translates into 1 kW peak power (50 V× 20 A);
- Adjustable output quiescent voltage.

Figure 3.12 shows the schematic of the drain pulser. It includes a non-inverting amplifying stage followed by a driver-booster OpAmp configuration with a power output stage. The booster OpAmp, an *APEX* PB63, allows high voltage excursions[1] with a high slew-rate of 1000 $V/\mu s$. The total voltage gain, 30 V/V, is split between the first OpAmp, 3 V/V, and the driver-booster OpAmp, 10 V/V, and a very high current capability is provided by the output stage through high power Metal-oxide-semiconductor FETs (MOSFETs).

The drain pulser can be divided in 3 sub-circuits: a low voltage amplification with stable reference stage, a high voltage summing amplifier stage and an output class AB buffer stage. The first voltage amplification stage is based on a fast LM7171 OpAmp used in a non-inverting configuration such that its gain was 3 V/V. This stage was used to split the total required gain of 30 V/V and to allow an easier 50 Ω input match. Additionally, a *zener* diode/potentiometer combination was used as voltage reference instead of the more stable and precise voltage reference integrated circuit (IC) used in the gate pulser. The *zener* diode reference was accurate enough for the intended measurements since the quiescent voltage, i.e., the "pulsed-off" level, could also be set directly through the AWG. Furthermore, having 0 V at the drain is not as potentially harmful as at the gate.

[1] The PB63 manufacturer recommended supply voltages range from ± 20 V up to ± 65 V.

Voltage amplification and extended excursion is provided by the high voltage amplification stage which consists of a composite amplifier built with a low voltage LM7171 OpAmp and an *APEX* PB63 power OpAmp.

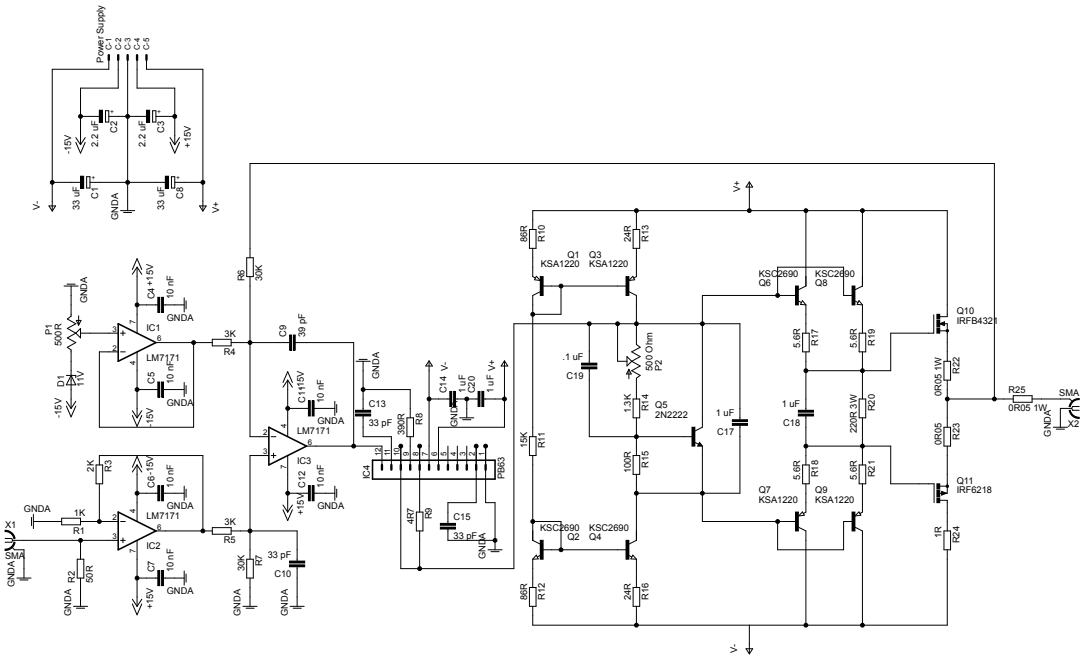


Figure 3.12 Drain pulser circuit schematic.

Since the output buffer stage, which was built with discrete transistors, may be considered transparent in terms of the voltage signals in the circuit, the composite amplifier can be regarded as a difference amplifier with $R4$, $R5$, $R6$ and $R7$ defining the weights or gains as follows:

$$V_{OUT} = \frac{R6}{R4} \cdot (V_{IN} - V_{REF}), \tag{3.2}$$

with $\frac{R6}{R4} = \frac{R7}{R5}$. The reference voltage used, V_{REF}, ranged from -4 V to 0 V. But, since it is applied at the negative port of the difference amplifier, it adds up to the pulse voltage applied at the other port. The *APEX* PB63 was added to the design such that voltage amplification and higher voltage excursions, up to approximately[2] 55 V were achieved. Besides the high voltage capabilities, this power OpAmp also has a reasonably high output current capability of 2 A. In Figure 3.13, the PB63 is drawn as a 12-pin device. Pins 6 and 7 are the supply inputs and

[2]Since the power OpAmp, the PB63, is not of the rail-to-rail type, the output voltage saturates at 10 V below/above the positive/negative supply, which results in 55 V maximum output voltage.

the first 5 pins as well as the last 5 belong to each of the two OpAmps that are included in the same 12-pin package. Only one of the packaged OpAmps was used in the design of the pulser. Table 3.1 describes all of the device pins and how they were connected.

Pin Nr.	Pin Name	Description
1/12	IN	Input pin 12 is connected to the output of the driver and pin 1 to ground to prevent input/output floating.
2/11	COMP	Compensation pins both connected to a 33 pF capacitor as recommended by the manufacturer.
3/10	OUT	Where the voltage at the current limit resistor is fed to the over-current protection circuitry.
4/9	GAIN	Gain of the PB63 set according to: $Gain = 1 + \frac{2000}{R_{gain}}$, access to the internal negative feedback.
5/8	R_{lim}	"Real" PB63 output where current limit resistor is connected, $I_{lim} = \frac{0.7}{R_{lim}}$.
6	$+V_s$	Positive power supply bypassed by electrolytic, 33 μF, and ceramic, 1 μF, capacitors.
7	$-V_s$	Negative power supply, bypassed similarly .

Table 3.1 Power OpAmp PB63 pin use and description.

The total gain of the driver-booster amplifier is 10 V/V and a 390 Ω resistor was used at the GAIN pin setting the booster OpAmp to approximately 6.1 V/V, thus, leaving the remaining needed voltage gain to the driver OpAmp. This gain distribution was a compromise between several factors:

1. the driver stage output voltage does not get close to the supplies, i.e., dividing the maximum output swing of this stage, 55 V, by the booster gain, 6.1 V/V, results in roughly 9 V maximum output swing for the driver which is far enough from the ± 15 V rails;
2. stability is more difficult to achieve as the driver gain approaches 1;
3. the gain-bandwidth product of the driver should be kept lower than the closed loop bandwidth of the booster, which means that not too high gain is desirable at the booster. To decrease the driver gain-bandwidth, a 39 pF capacitor, $C9$, was used;
4. the used booster gain remains inside the manufacturer recommended range, 3 to 25;

Since, even with care in its design, the overall circuit still had some stability issues, a 33 pF was added, $C10$. This capacitor made the overall circuit gain start to decrease at lower frequencies, by creating a pole at a frequency approximately given by:

$$f_c = \frac{1}{2\pi \cdot C10 \cdot R7 \,//\, R5} = \frac{1}{2\pi \cdot 33\,\text{pF} \cdot 3\,\text{k}\Omega \,//\, 30\,\text{k}\Omega} \approx 1.75\,\text{MHz}. \tag{3.3}$$

So far, two main high level blocks of the drain pulser circuit have been described. The last one, the output stage, shown in Figure 3.16, can itself be sub-divided into three smaller parts: current reference/mirror and the V_{be} multiplier, the BJT driving stage and the output power MOSFETs. The output stage high power MOSFETs have very high input capacitance, on the order of thousands of pF's. This means that, considering the MOSFET gate as a single capacitor generally described in terms of its voltage-current relation:

$$i_C(t) = C \cdot \frac{dv(t)}{dt}, \tag{3.4}$$

and assuming that $i_C(t)$ has a constant peak value, the MOSFET gate charging current equation can be expressed as:

$$I_C = C \cdot \frac{\Delta V}{\Delta t}, \tag{3.5}$$

which means that, to have a 30 V pulse with a 0.1 µs rise time on a 5000 pF input capacitance MOSFET, the required slew rate is 300 V/µs and the current needed can be calculated according to:

$$I_C = 5000\,\text{pF} \cdot \frac{30V}{0.1\mu\text{s}} = 1.5\,\text{A}. \tag{3.6}$$

Hence, a very high peak current of 1.5 A is needed to avoid limiting the slew rate at the MOSFET's gate and consequently at its output. Therefore, a very high peak current capability is needed at the previous stages for the proper driving of the output transistors. The MOSFETs biasing current was adjusted with the V_{be} multiplier potentiometer being measured through voltage drop at the resistor $R24$, added just for that purpose. The BJTs were selected accordingly to the needed voltage ratings and with f_T's above 200 MHz. The used MOSFETs are intended for high speed high current switching as well.

The V_{be} multiplier is biased through the current reference/mirror made up with the transistors $Q1$, $Q2$, $Q3$ and $Q4$ plus the resistors $R10$, $R11$, $R12$, $R13$ and $R16$. The reference current can be defined, considering $R10 = R12$ and $R13 = R16$, according to:

$$I_{REF} = \frac{(V_+ - V_-) - 2 \times V_{BE}}{R11 + 2 \times R10}, \tag{3.7}$$

assuming that V_{BE} is constant and equal for NPN and PNP transistors. Thus, the reference

current is mirrored or replicated with a multiplication factor approximately given by the ratio of R10 to R13. Considering that the $Q1$, $Q3$ and the $Q2$, $Q4$ pairs are well matched, the BJT has high current gain: $\beta \to \infty$ and neglecting the Early effect, the reference current, I_{REF}, and the mirrored current which will bias the V_{be} multiplier, I_O, are given by:

$$I_{REF} = I_S \cdot exp\left(\frac{V_{BE}}{V_T}\right), \tag{3.8a}$$

$$I_O = I_S \cdot exp\left(\frac{V_{BE} + I_{REF} \cdot R10 - I_O \cdot R13}{V_T}\right), \tag{3.8b}$$

and taking the ratio of both expressions:

$$\frac{I_{REF}}{I_O} = exp\left(\frac{I_{REF} \cdot R10 - I_O \cdot R13}{V_T}\right), \tag{3.9}$$

which, after some simple manipulations, results in:

$$\frac{I_{REF}}{I_O} \cdot \left(\frac{V_T}{I_O R_{13}} \cdot ln\left(\frac{I_{REF}}{I_O}\right) + 1\right) = \frac{R10}{R13}. \tag{3.10}$$

Equation (3.10) is not easily solvable for just one of the currents but looking closely at the logarithm, if the ratio between I_O and I_{REF} is not too large , e.g., below 5, and considering the multiplication with the factor $\frac{V_T}{I_O R_{13}}$, with V_T approximately equal to 25 mV at room temperature, if $R_{13} I_O \gg V_T$ one can approximate:

$$\left|\frac{V_T}{I_O R_{13}} \cdot ln\left(\frac{I_{REF}}{I_O}\right)\right| \ll 1 \quad \Rightarrow \quad \left(\frac{V_T}{I_O R_{13}} \cdot ln\left(\frac{I_{REF}}{I_O}\right) + 1\right) \approx 1, \tag{3.11}$$

which leads to:

$$\frac{I_O}{I_{REF}} \approx \frac{R10}{R13}. \tag{3.12}$$

This means that the ratio of the currents in the current mirror is indeed approximately equal to the ratio of the emitter resistors. With the resistor values used, Figure 3.13, according to Equations (3.7) and (3.10), the reference current[3] is set around 5.5 mA.

With the emitter resistors ratio of 3.6 the bias current through the V_{be} multiplier becomes approximately 20 mA. The emitter degeneration resistors at the current mirror were allowed the use of a smaller reference current and, most of all, served to provide thermal stability.

[3]The reference current depends on the supply voltages used and the currents calculated correspond to $+V_s =$ 65 V and $-V_s = -20$ V. Considering the entire recommended operating range of the PB63, the reference current range may vary between 2.5 mA and 8.4 mA.

Even with the thermal coupling given by the placement of the BJT pairs on the same heatsink, without these resistors, the circuit would suffer from in "thermal runaway".

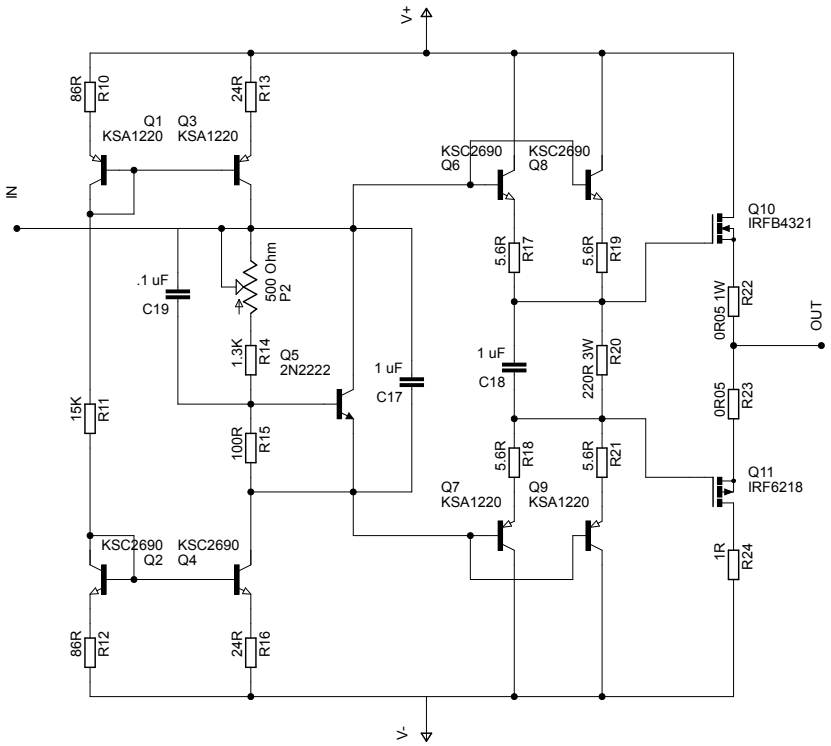


Figure 3.13 Drain pulser output stage circuit schematic.

The bias current of the V_{be} multiplier can flow through two paths: through the resistors $R14$, $R15$ and $P2$ and through the transistor $Q5$. Neglecting the current through $Q5$ base, the current through the resistors is given by $\frac{V_{BE}}{R15}$ and, assuming $V_{BE} \approx 0.65$ V, it becomes 6.5 mA. Therefore, the remaining 13.5 mA served to bias the $Q5$ transistor. The V_{be} multiplier ultimate purpose is to bias the output MOSFETs $Q10$ and $Q11$, although it also indirectly biases the emitter followers $Q6$ to $Q9$. It can be regarded as a voltage source whose output value is approximately calculated as:

$$V_{O_{Vbe}} = V_{BE} + \frac{V_{BE}}{R15}(R14 + \alpha \cdot P2), \qquad 0 \leq \alpha \leq 1, \tag{3.13}$$

where α represents the variable resistance of the potentiometer, which is manually adjustable. Through that, the voltage across the V_{be} multiplier can be set to any value between 9.1 V and 12.35 V. The capacitor $C17$ was used to bypass higher frequencies and the feedback through $C19$ to improve stability.

Transistors $Q6$ to $Q9$ are biased by the V_{be} multiplier and the resistor $R20$. The V_{be} mul-

tiplier was designed such that each of these transistors were biased at approximately 20 mA. Once more, a bypass capacitor, $C18$, was used. Additionally, the emitter resistors $R17$, $R18$, $R19$ and $R21$ served to properly balance the bias currents through the parallel BJTs. Although the PB63 has high current capability, the use of a 4.7 Ω current limit resistor prevented it from exceeding 150 mA. Thus, the $Q6$ to $Q9$ transistors were used as buffers to avoid stressing the PB63. Two parallel BJT were used in order to allow, not only higher current peaks, but also a smaller resistance value for $R20$, which lowers the output impedance of the buffer.

Agilent ADS was used to simulate the drain pulser circuit, Figure A.2 in Appendix A. The simulation results of the drain pulser when driving a low resistive load, 10 Ω and an available model of a medium power GaN HEMT from *Cree, Inc.* biased at a high V_{GS}, such that its drain to source conductivity is high, are depicted in Figures 3.14 and 3.15.

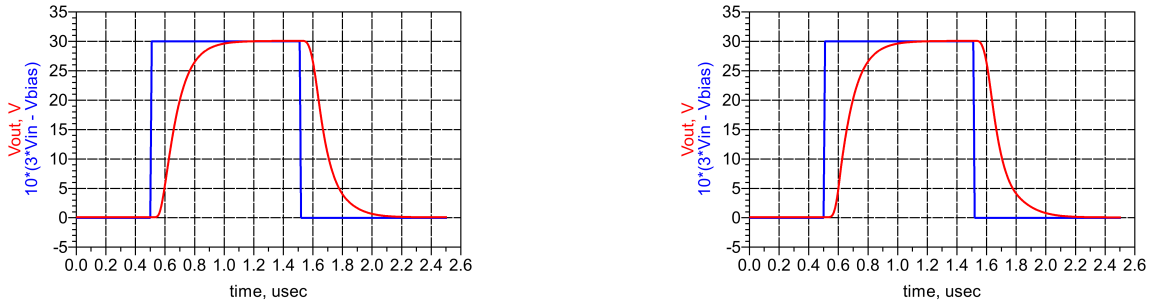


Figure 3.14 Drain pulser simulation input and output voltage pulses. Left: 10 Ω load resistor. Right: 15 W GaN HEMT model biased at $V_{GS} = 0$ V DC.

Figure 3.14 shows that the input and output voltages with the resistor and the transistor model are practically identical. However, in Figure 3.15, the current pulse behaviour is not as well behaved as in the resistor case where it obviously follows the voltage pulse.

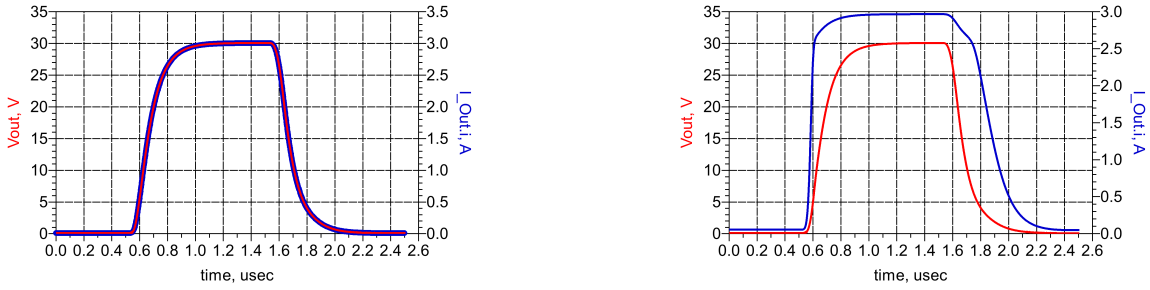
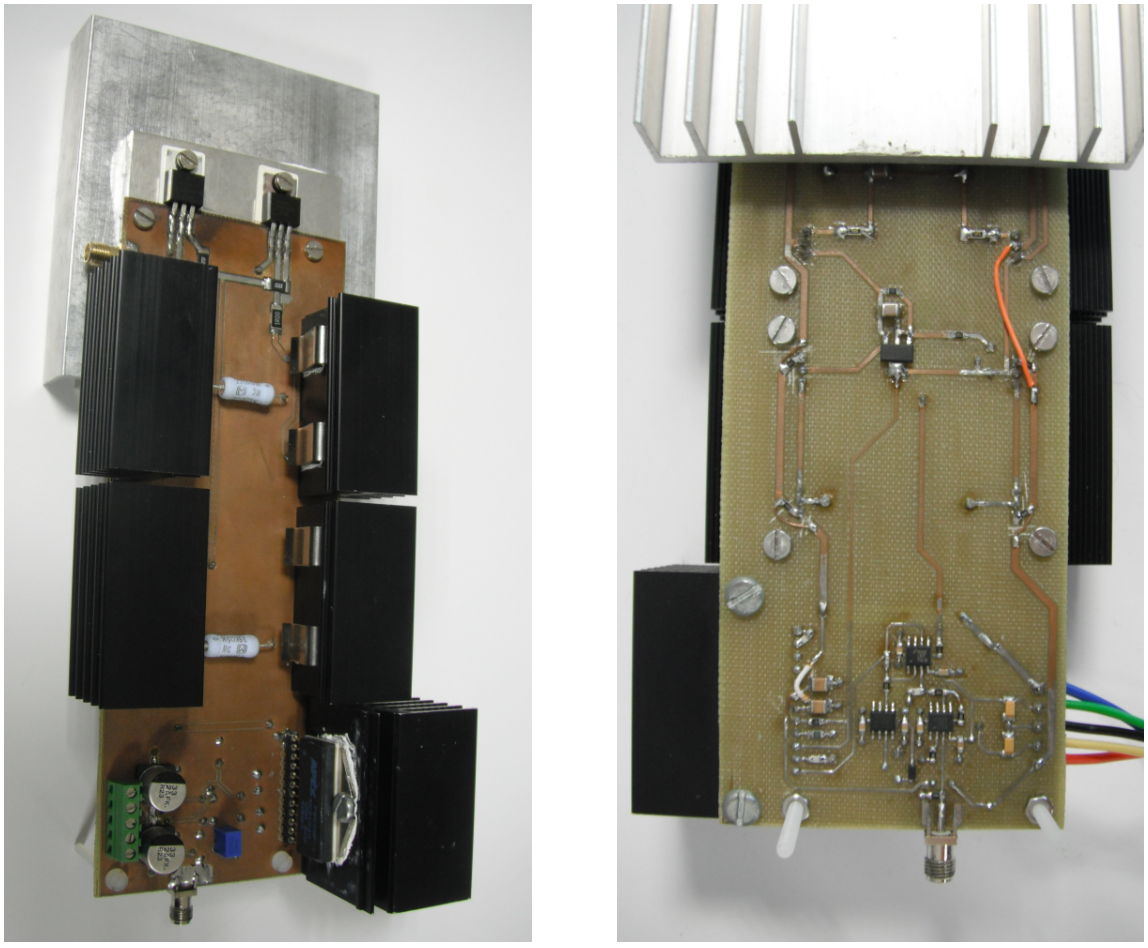


Figure 3.15 Drain pulser simulation output voltage and current pulses. Left: 10 Ω load resistor. Right: 15 W GaN HEMT model biased at $V_{GS} = 0$ V DC.

Nevertheless, the overall specifications in terms of speed and current and voltage amplitudes were met in the simulations and the next step was the practical implementation of the pulser.

The drain pulser was implemented in a PCB shown in Figure 3.16. As mentioned before, appropriate heat-sinks were used since, even with low bias currents, the high supply voltages generate a considerable amount of power that needs to be dissipated.



(a) Bottom view. **(b)** Top view.

Figure 3.16 Drain pulser PCB implementation.

A test was performed to the drain pulser with a 12 Ω load, from which the measured voltage and current waveforms are shown in Figure 3.17. Input pulses duration was 10 µs. Similarly to the gate pulser, fall and rise times are controlled by the pulses generated at the AWG. Sufficiently short rise and fall times are desirable. However, if they are too short, the output pulse will not be able to follow the input, and excessive ringing appears at the output pulse. Note that the pulse voltages do not correspond exactly to the nominal values, which means that, in order to obtain very accurate pulsed voltages, a gain calibration is needed for the drain

pulser, similarly to what happened to the gate pulser.

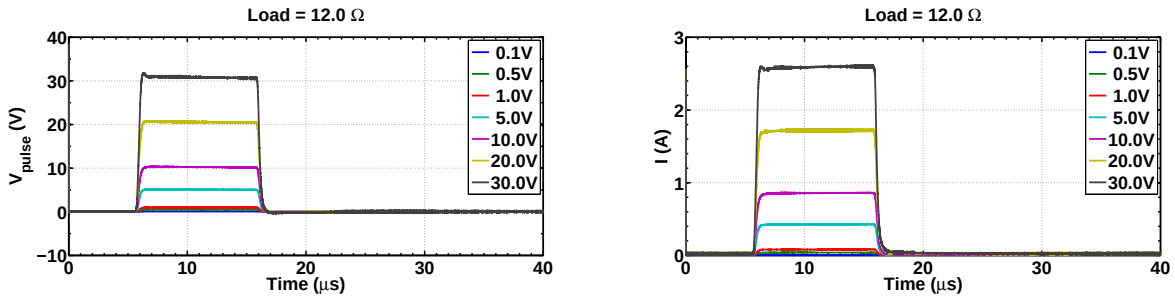


Figure 3.17 Drain pulser response to a 10 μs pulse loaded with a 12 Ω resistor. Left: Output voltage. Right: Output current.

3.4 Pulsed I-V Measurement System

Previous section described the gate and drain pulsers and how they were developed. The pulsed I-V measurement setup was built with these circuits and several laboratorial equipment, as briefly described earlier in this chapter. In the following paragraphs the most relevant features of this measurement setup will be described as well as its high level block architecture and measurement time diagrams.

3.4.1 DUT Testbed

The DUT was placed on a test-bed of a thick aluminium plate, which served as mechanical support and heat-sink. The test-bed input and output ports were connected to bias-tees dedicated to pulsed measurements, Figure 3.18.

The voltage was measured either at the drain or gate pads as close as possible to the DUT pads. Although placing a voltage probe at the gate or drain ports does not affect the low frequency pulsed measurements, it may cause oscillations due to its parasitic capacitance, which was approximately 8 pF. The use of the bias-tees avoided oscillations caused by possible feedback loops between the device, the pulser and the power-supply. However, pulsed DC measurements could be performed without these. If pulsed S-parameters are required though, the bias-tee becomes indispensable.

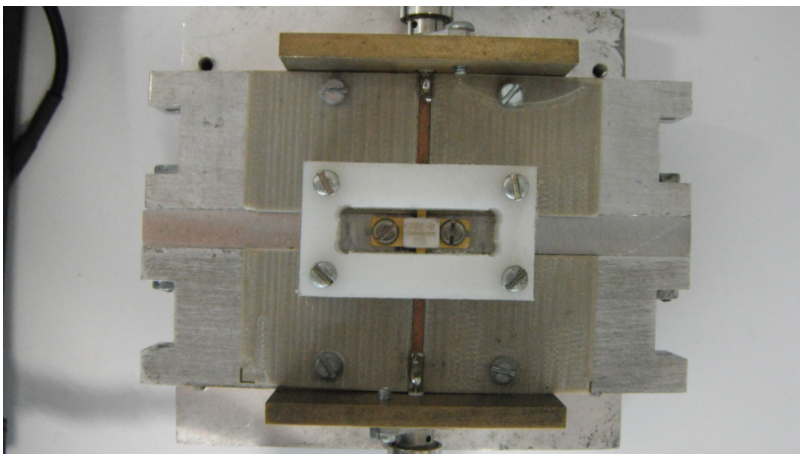


Figure 3.18 DUT test-bed.

3.4.2 Pulsed DC Bias-Tees

To perform pulsed measurements through the bias-tees DC port, and maintain pulse integrity, specific bias-tees are needed [43]. Namely, a sufficiently high DC port bandwidth is crucial, such that the pulse shape is minimally affected as it passes through the bias-tee. The 8860S model from *Aeroflex/INMET* was found to be a cost-effective solution regarding pulsed DC bias-tees and was, therefore, added to the measurement setup. Since only pulsed DC measurements were performed, the RF ports were terminated with 50 Ω loads. Figure 3.19 shows the bias-tee model used in the measurement setup. The manufacturer specified its frequency behaviour in terms of insertion loss from the DC and AC ports to the AC+DC port.

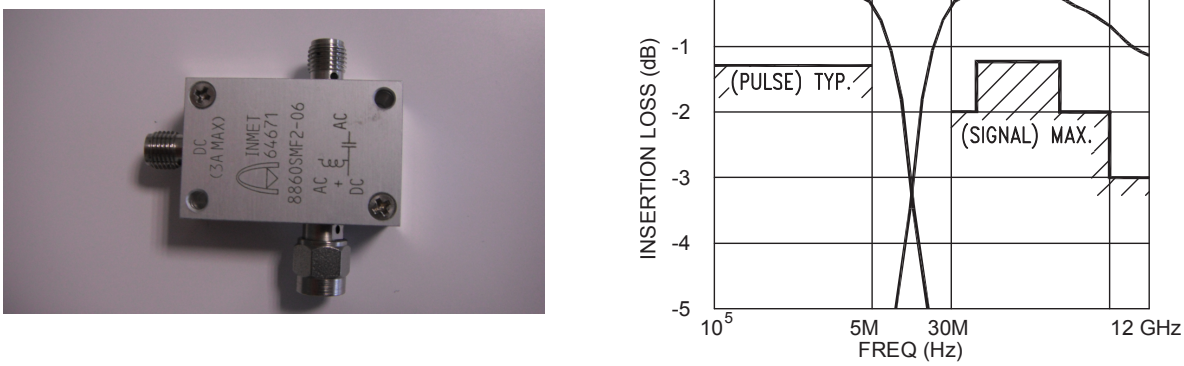


Figure 3.19 Left: Aeroflex/INMET 8860S pulsed bias-tee. Right: pulsed bias-tee DC to RF+DC and AC to RF+DC insertion loss, reprinted from [44].

The 5 MHz bandwidth of the DC port was high enough and, thus, the bias-tee have minimal impact on voltage pulses as short as 1 μs or even less. For instance, assuming a dominant single pole response characteristic of the bias-tee DC to RF+DC port, the rise time would be given by:

$$\tau \approx \frac{0.35}{BW} = \frac{0.35}{5\,\text{MHz}} = 70\,\text{ns}, \tag{3.14}$$

which means that, since the shortest rise and fall time of the pulsed voltage waveforms was 200ns, the DC path bandwidth was sufficiently high and, thus, the bias-tee had minimal impact on those signals. In a pulsed I-V/RF measurement system the bias-tee is one of the limiting factors among all of the setup hardware [45]. Hence, its careful selection or design is an important step when building a pulsed measurement environment.

3.4.3 SMA/DC Cables

For the pulsed gate measurements, an SMA to DC-plug coaxial cable was used to connect the bias-tee DC port to the power supply that controlled the DC drain voltage. The drain current was measured with the TCP0030 current probe clamped to the isolated conductor wire of the SMA to DC cable.

The measurements with the drain pulser required a different cable, an SMA to SMA but with an isolated central conductor such that the current flowing through it could be measured. This was done due to the fact that the drain pulser output and the bias-tee DC input are interfaced through SMA connectors. Therefore, a common SMA coaxial cable had to be modified and a short section of it was converted into a bifilar line as shown in Figure 3.20.

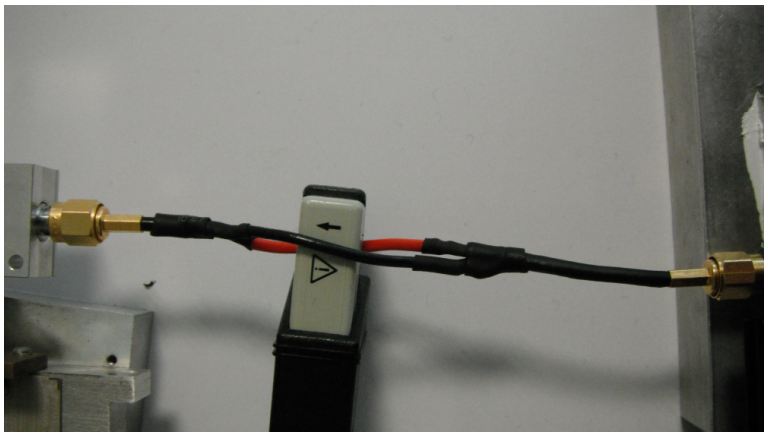


Figure 3.20 Current probe, TCP0030, clamped to the modified coaxial cable.

The SMA connectors and coaxial cables were used to better preserve pulse integrity. The modification of a short section of the coaxial cable had almost no impact in the performed measurements, given that the bandwidth requirements were just a couple of MHz.

3.4.4 Measurement Setup Diagrams

Two measurement setups were built including the elements previously described: one setup dedicated to measurements with the gate pulser only and another to the drain pulser. The setup diagram shown in Figure 3.21 was used to perform pulsed measurements with the input excitation pulse at the gate of the DUT. The voltage at the drain of the device was set to a DC value through the MATLAB script that was controlling the measurement process.

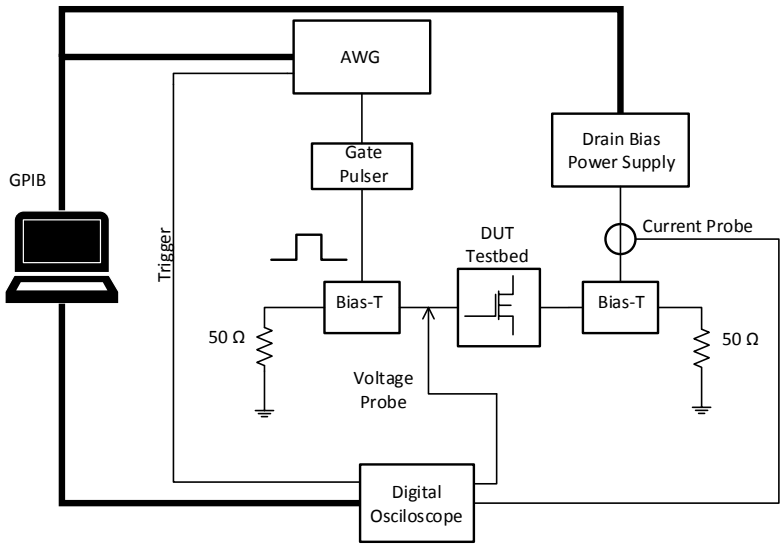


Figure 3.21 Setup diagram for pulsed I-V curves extraction using the gate pulser.

The setup becomes slightly different when performing pulsed measurements with the input voltage pulse at the drain, Figure 3.22. The drain current is no longer supplied directly by the power supply but through the pulser circuit. The current probe that was used was precise enough and reached sufficiently high frequencies, up to 120 MHz, which was way beyond the required measurement bandwidth. An alternative to the current probe is to use a current sense resistor. However, its dynamic range would be limited, depending on the resistor value and the current values to be measured.

Figure 3.23 shows the laboratorial pulsed I-V measurement setup that was implemented for the realization of pulsed drain measurements. Three power supplies with two outputs each

were used, resulting in 6 DC outputs: four of these to set the two positive and two negative voltages of the drain pulser, one for setting V_{GS} and one to power up the cooling fan.

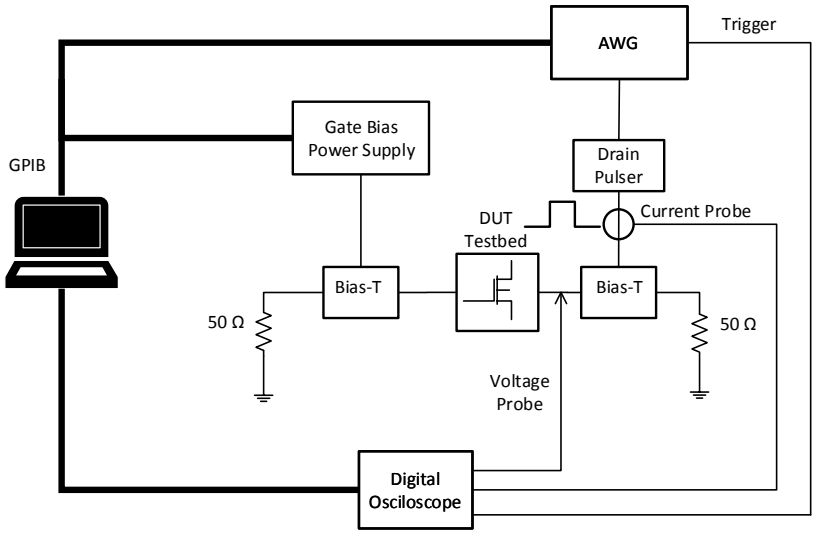


Figure 3.22 Setup diagram for pulsed I-V curves extraction using the drain pulser.

A close-up of the measurement apparatus closer to the DUT is shown in Figure 3.24. The oscilloscope voltage probes were hooked to a pin that was soldered onto the microstrip line of the test-fixture and the current probe measured the drain current, flowing through the modified coaxial cable, which was provided by the drain pulser.

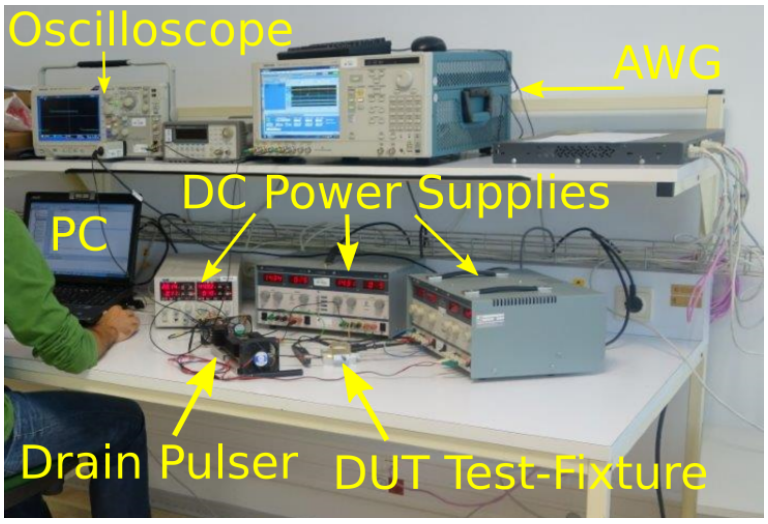


Figure 3.23 Pulsed I-V measurement setup implemented at the Telecommunications Institute RF laboratory.

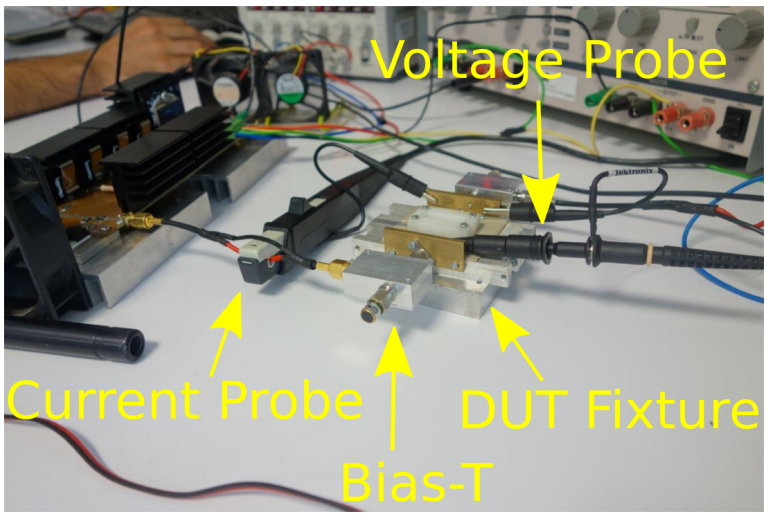


Figure 3.24 Close-up view of the test-bed and drain-pulser when performing measurements.

3.4.5 Data Acquisition and Processing

As mentioned earlier the system can, in a single run, and without external intervention, acquire time-domain current and voltage waveforms for any range of drain/gate pulses and gate/drain DC biases, just limited by gate and drain pulser electronics and available supply voltages. From that measured time-domain data, I-V plots can be drawn within the MATLAB environment according to the sampling times and periods that one may select.

The measurement software has two main loops. The first one sweeps the DC bias at the drain or gate and, inside that loop, pulse waveforms are loaded and outputted by the AWG such that the desired gate or drain pulse is generated at the DUT. To guarantee that the measurement oscilloscope is always synchronized, the AWG generates a trigger signal, as depicted in Figure 3.25. This guarantees measurement synchronization independently from the input pulse voltages. Furthermore, the collected waveforms are first averaged by the digital oscilloscope to increase its signal to noise ratio (SNR). Given the very low duty cycles, as low as 0.01 %, necessary to keep the DUT under isothermal or quasi-isothermal conditions, this average processing can increase dramatically the measurement time. For example, considering 20 points of V_{DS}, 10 points of V_{GS} with 10 averages and a pulse repetition time of 500 ms, a simple calculation results in at least 34 minutes[4]. However, the data-acquisition and setting

[4]The calculation results from: $\frac{20\,\text{pts}\times 10\,\text{pts}\times 10\,\text{avg.}\times 0.5\,\text{s}\times 2\,\text{ch.}}{60\,\text{s}}$. The multiplication by 2 is due to the oscilloscope acquisition of just one channel at a time.

of the bias are not instantaneous and more than 10 averages may be required. This can ultimately lead to a couple of hours or more to extract an accurate pulsed DC I-V plot.

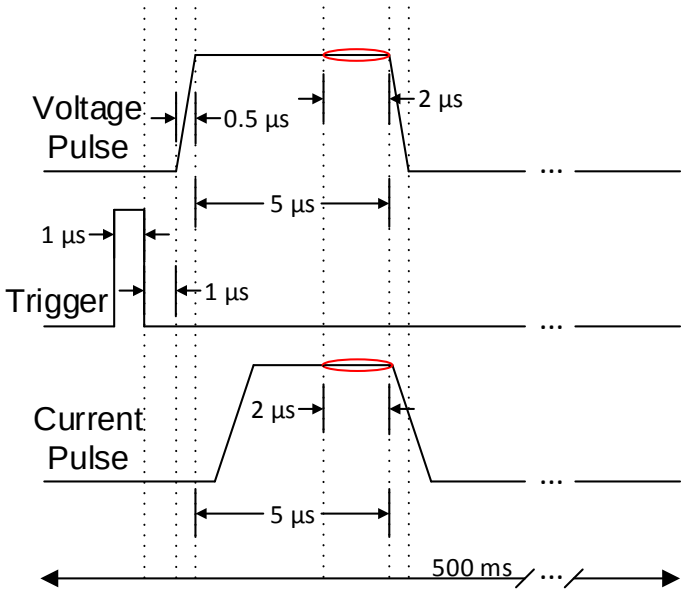


Figure 3.25 Example of a pulsed I-V measurement temporal diagram.

In Figure 3.25, the time intervals contained inside the red ellipse represent the measurement samples that were used to build the final I-V plot. Measurement samples were collected only inside a time slot at the end of the pulses to avoid any transient effects and to guarantee that either voltage and current pulses settled to steady values. This regions contained up to thousands of samples which were averaged to obtain a single voltage or current value for each different pulse and bias. Hence, to get the final current and voltage values used to plot I-V curves, the collected data was not only averaged during measurements at the oscilloscope, but also during its processing when creating the I-V plot.

Chapter 4

GaN HEMT LTME due to Trapping

With the two pulsed I-V measurement setups described in Chapter 3, one can extract quasi-isothermal I-V curves of GaN HEMTs or, virtually, of any transistor. Furthermore, with the appropriate stimulus/measurements, it was possible to observe and characterize long term memory effects typically exhibited by GaN devices. These effects are known to degrade considerably the performance of RF and microwave PAs and reduce the effectiveness of pre-distortion linearizers [46], being a major topic of research for PA designers and device model developers.

4.1 What are LTME?

Memory effects in the context of RF PAs started drawing the attention of the academic and scientific world on the late 1980s [47]. The term was, however, first proposed by Chua [48], regarding the influence on the output of a non-linear system at time t by the input(s) not only at time t but also spanning the past history up to some instant $t-\tau$. This also means that we typically consider a fading memory, i.e., that the influence of the input(s) at the more distant past, previous to $t-\tau$, on the output of the system fades to zero. Ultimately, the term memory-effects is just a short way to mention all the dynamics of a device or system, like an RF power transistor.

Within the RF power amplifier domain it is usual to divide memory effects in two groups based on their time span: short and long memory effects. Short-term memory effects manifest themselves within a time window of the scale of the RF signal period. On the other hand, when the observed memory effects on the circuit/device occur on time-scales much longer than the RF carrier, they are designated LTME. Figure 4.1 shows the most common sources of both long

and short-term memory effects in a transistor circuit. Those sources can be further divided in two categories according to their origins: the transistor itself and the external matching and biasing circuitry.

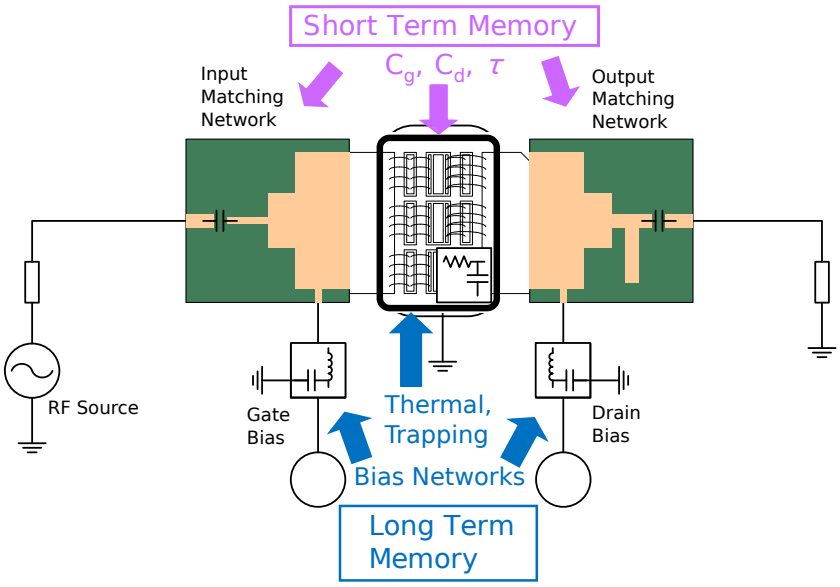


Figure 4.1 Long and short-term memory effects sources in a transistor circuit, adapted from [49].

Short-term memory effects include the high frequency dynamics of the RF transistor originated by its associated reactances, either from its intrinsic part, caused by the device's charge storage mechanisms, or its extrinsic part, i.e., the parasitics of the device. Inductors and capacitors are usually good enough to describe the dynamics of the extrinsic components or parasitics, which are typically regarded as linear and thus, bias-independent. The intrinsic charge storage mechanisms are typically non-linear, and dependent on the instantaneous voltage/current at the device. However, when linearised at each bias-point these can be modelled as constant capacitances. In this way, at small-signal the short-term memory effects of the device are just the set of its bias-dependent frequency responses. When large-signal operation is considered, the relation between the voltage/current at the device and the charge stored becomes crucial as it will allow the prediction of the gain compression (AM-to-AM) and phase transfer characteristic (AM-to-PM) of the overall PA/System more accurately. The matching networks constitute another major source of memory effects which are included in the short-term category. Another source of short-term memory effects, according to [13], is the interaction between the transistor and the output matching network, since the latter is not designed to present a conjugate output match but the optimum load for maximum output power, efficiency, or a compromise between these two. Thus, reflections will result and under

large-signal the reflection coefficient at the output of the device becomes what is known as the *hot*-S_{22} [50].

Long-term memory effects are typically caused by: DC bias networks, thermal effects and trapping effects. The bias networks provide a low impedance path for DC up to a few MHz, the so-called video bandwidth, while presenting a high impedance for RF signals. To control the video bandwidth, reactive elements are used, whose long time constants will affect the low-frequency dynamics of the overall PA, introducing long-term memory effects. One very interesting consequence of the non-zero impedance of the DC path at low frequencies will be their impact on the third-order IMD (IMD3). Despite baseband components are generated in even-order non-linearities, these will then experience the non-zero impedance in the video-bandwidth and slowly modulate the bias-point of the device at the envelope time-scale. This modulation will produce a *re-mixture* of the RF carrier with the baseband and will then be noticeable in the IMD3, particularly in its asymmetries [51].

Thermal phenomena are a major source of long-term memory effects. Hence much effort is put into the thermal characterization of the RF transistors and the inclusion of this effects in the corresponding models. A practical approach for including these effects is the use of an equivalent R-C network that mimics the temperature in the channel of the transistor, together with a scaling function whose input is the R-C output voltage representing the temperature, which modifies the non-linear drain current as already mentioned in Chapter 2. The time constants normally associated with temperature are very large when compared to the RF signal periods, from μs to ms, which make them very slow effects when compared to other memory sources. Figure 4.2 shows the "spread" around the mean AM-to-AM and AM-to-PM curves caused by long-term memory effects, including temperature.

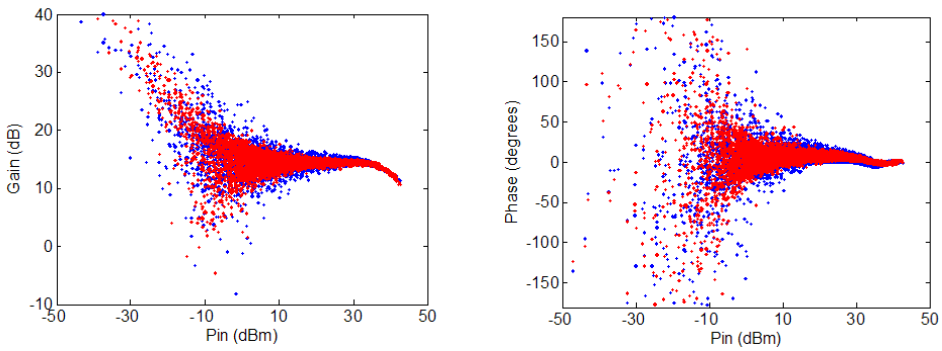
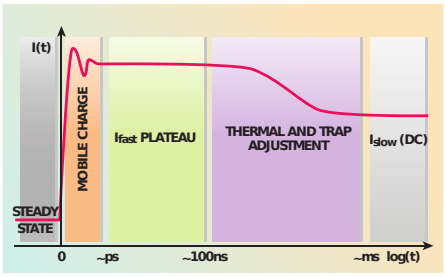


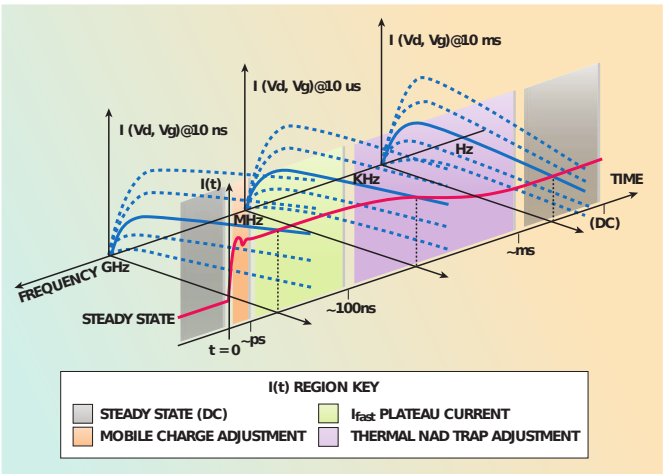
Figure 4.2 Dispersion in the AM-to-AM and AM-to-PM curves from a 400 W Doherty PA using a wideband code-division multiple access (WCDMA) signal. Blue: Measured, Red: Modeled, reprinted from [52].

Wide band-gap, III-V, RF power transistors technologies like GaAs and GaN also shows another type of long-term memory effects, caused by trapping states in the semiconductor materials. These are included in the long-term memory effects group due to their associated very long time constants.

Figure 4.3 shows how all types of memory effects change the I-V curves of a FET when DC and pulsed measurements are used for their acquisition. It is clearly visible that for different frequencies/time periods the I-V curves change dramatically and the device model needs to accommodate these changes. For instance, the I-V curves for the DC measurement have a negative slope of the I_{DS} current versus V_{DS} in the saturation region, which would lead to a negative output resistance, R_o, contrasting with what is typically seen in I-V curves of transistors in general whose output resistance is usually rather large and positive. This is caused by the temperature at the device. Since it is characterized with DC stimuli, the temperature will change from point to point in the I-V curves resulting in non-isothermal curves. It is not even possible to fully characterize the device under this conditions without irreversibly damaging it or even destroying it, given the high power being dissipated at the upper-right corner of the I-V plane(very high V_{DS} and I_{DS}). The I-V curves will change with different temperature conditions, as well as other related device characteristics, like the small signal transconductance, g_m, which will be affected as well with temperature variations.



(a) Response versus time $I(t)$.



(b) Response versus input voltages $I(V)$ or I-V curves.

Figure 4.3 Representative current response when voltage pulses of different time widths are applied at the gate or drain terminal of an RF FET, reprinted from [53].

In the following section the charge carriers trapping phenomena and its practical implications in the development of device models and PA design will be discussed in more detail.

4.2 Trapping Effects in GaN HEMTs

In Figure 4.4, the general structure of a GaN HEMT device is depicted. HEMTs operating principle is similar to a general FET in the sense that its output drain current is controlled by the applied gate voltage: $I_{Drain} \propto V_{Gate}$. However its internal structure and production process is particularly different from Silicon LDMOS technologies or GaAs MESFET, where, for example, hetero-junctions are not built and so there is no formation of the 2DEG, as briefly addressed in Chapter 1. Due to the lack of GaN substrates other materials are used, usually SiC, Si or sapphire, for very high-performance applications. The conduction channel in the GaN HEMT is created in the 2DEG, first reported in literature by Kahn et al. [54], which is generated below the GaN/AlGaN hetero-junction. The difference between the lattice constants of the substrate layers and those of the GaN buffer layer pose some difficulties in the device fabrication and cause what is called lattice dislocations being also one of the main causes for the trapping of charge carriers [55].

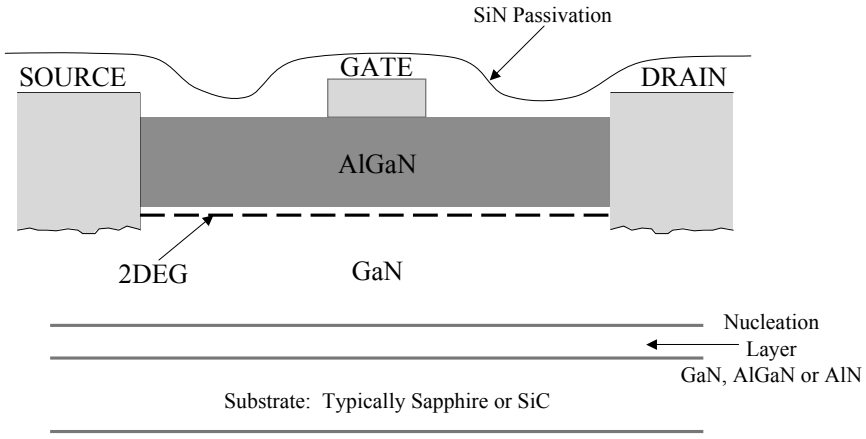


Figure 4.4 GaN HEMT simplified physical structure, reprinted from [56].

There are mainly two different origins for the trapping of charge carriers inside wide bandgap devices such as GaN HEMTs, usually referred in literature: surface states traps and buffer traps, Figure 4.5. Although there is still research undergoing about these phenomena, as they are still not completely understood and characterized, surface traps are mostly associated with gate-lag effects and buffer/bulk traps to drain-lag. Recent developments in the production process of GaN devices tend to mitigate the gate-lag effects: *passivation* layers, field plates and changes in the structure beneath the gate. However, drain-lag effects are still a major concern for PA designers and device modellers.

Passivation layers on the HEMT, are deposited at later fabrication stages in order to de-

crease the negative impact of charge carrier trapping on high frequency operation. Figure 4.6 shows the defects on the crystal of an HEMT with and without the modification proposed in [12], which consists of the addition of a recessed-gate structure beneath the gate of the HEMT. The otherwise severe cracks on the crystal surface become greatly mitigated leading to a significant reduction in surface-traps and thus current-collapse as well as gate-leakage.

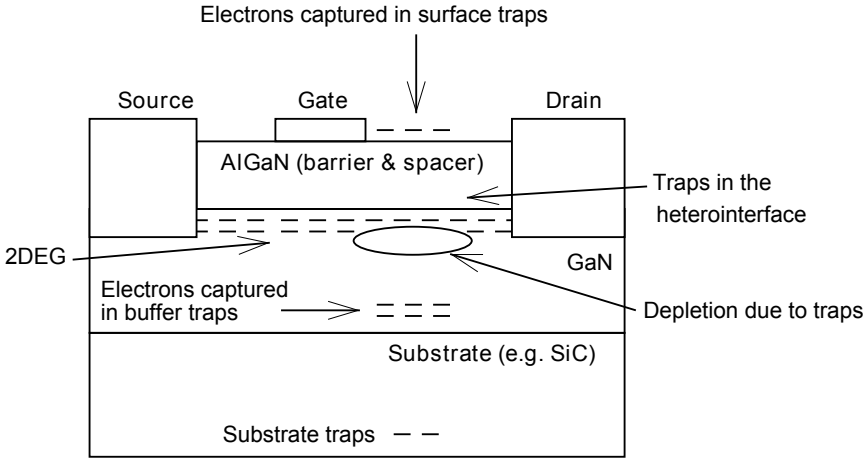


Figure 4.5 Trapping causes representation in GaN HEMTs, reprinted from [57].

Another often reported technique is the application of a source or gate connected field plate which was developed to mitigate surface-states related trapping effects as well as increasing the breakdown voltage [58]. The source-connected field-plate revealed to be a very good solution since it acted as a Faraday-cage, therefore reducing the reverse power transfer, S_{12}, while the gate-connected field-plate greatly increased C_{GD} capacitance and thus the *miller* effect [58], which negatively impacts the HEMT RF operation.

Even with the surface *passivation* technique, typically with silicon nitride (Si_xN_x) layers, and all the other methods successfully implemented in the production of GaN HEMTs, trapping-effects and consequently the associated long-term memory effects still significantly deter GaN technology from reaching its theoretical maximum performance. In fact, gate related memory effects have been greatly mitigated, but the bulk/substrate defects which are more related to drain-lag are yet to be fully corrected, which might be very difficult and take a long time. However, one can characterize, understand and carefully take into account those effects when producing a model or designing a PA.

Trapping effects are most noticeable in recent wide band-gap devices like GaN FETs despite having already been observed and studied during the development of the now more mature GaAs MESFET technology [59, 60].

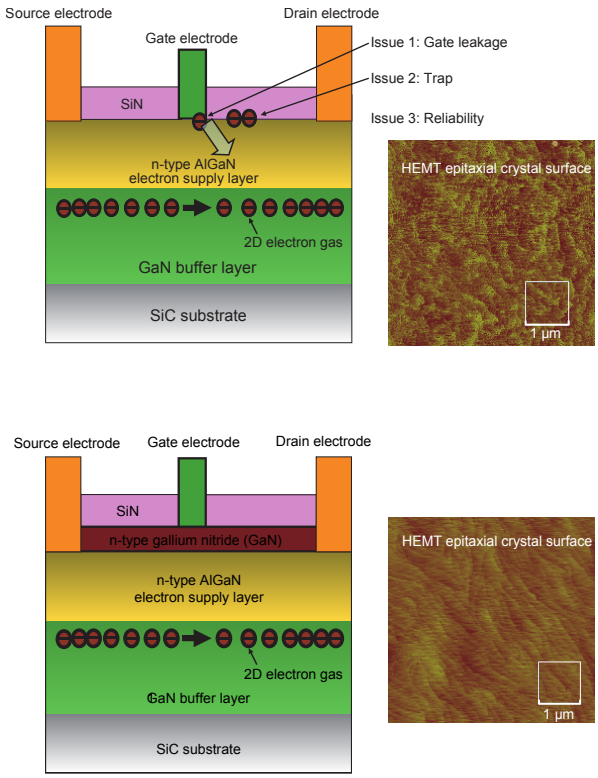


Figure 4.6 Comparison of HEMT structures: conventional HEMT versus an HEMT with a recessed-gate surface structure, reprinted from [12].

They also play a major role in the RF-to-DC dispersion and are responsible for effects such as current collapse, *knee-walkout* as well as transconductance and output conductance frequency dispersion. Figure 4.7 shows the impact of trapping effects on the I-V curves in what is described as *knee-walkout*. Since the theoretical maximum output power for linear operation can simplistically be given by,

$$P_{max,sat}^{lin} = \frac{I_{D_{SS}} \cdot (V_{br} - V_{Knee})}{8}, \tag{4.1}$$

where $I_{D_{SS}}$ stands for the maximum drain current, V_{br} is the breakdown voltage and V_{Knee} is the drain voltage at which the transistor leaves the triode or linear region and enters saturation, for the highest saturated current curve. Thus, given that trapping-effects dramatically impact the V_{Knee} voltage and the $I_{D_{SS}}$, the theoretical maximum output power is therefore degraded, despite the capability to handle higher junction temperatures, enhanced thermal conductivity and increased breakdown voltage of the GaN technology [61].

The trapping phenomena *per se* would be a less severe limitation to GaN HEMT based PAs if it did not have a dependency on the device terminal voltages. If charge carriers were cap-

tured and released within relatively equal time periods and these were of the same length of the RF signal period, the trapping and de-trapping processes would be contained and modelled within more common parasitic effects.

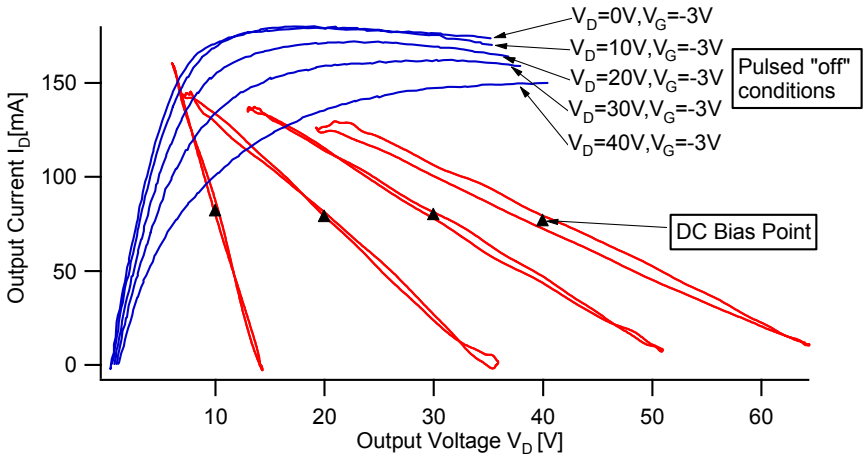


Figure 4.7 Knee-walkout and current collapse effect on optimum load-line for maximum output power in GaN HEMTss, reprinted from [62].

The PA performance would be slightly degraded when compared with an ideal device with no trapping effects. However, the trapping and de-trapping time constants typically observed in GaN HEMTs are far from being of the same order of magnitude. The longer time-constants, usually associated with de-trapping processes, can be as high as hundreds of milliseconds, and so of a higher length than typical signal carrier periods. On the other side, the shorter time constants, associated with the trapping phenomena, do not exceed the hundreds of nanoseconds barely reaching the microsecond range, which is much less than the former [63].

The asymmetry of the trapping associated time constants is therefore a major constraint to the device's optimal operation and consequently, on the overall PA performance, mostly if they are designed with models that do not include these effects. Besides the asymmetric time-constants, the trapping and de-trapping processes are highly dependent on the instantaneous electric fields at the device. The gate and drain voltages set the state of the trapping electrons in the device, which means that amount of memory observed depends on the input of the device.

Many challenges faced with the more recent GaN HEMT technology are already somewhat familiar to their users given the resemblance to the more mature GaAs technologies [64] provides a good overview about similarities and differences between both technologies regarding trapping effects.

4.3 Pulsed Gate I-V Measurements: Gate-Lag

The trapping and de-trapping time constants may be observed in the output current response when an appropriate pulsed stimulus is applied at either the HEMT gate or drain. When that voltage pulse is applied just to the FET's gate and its drain is biased at a DC voltage, if the drain current response to that gate stimulus takes a relatively large amount of time to reach the steady state, the transistor is said to be affected by gate-lag.

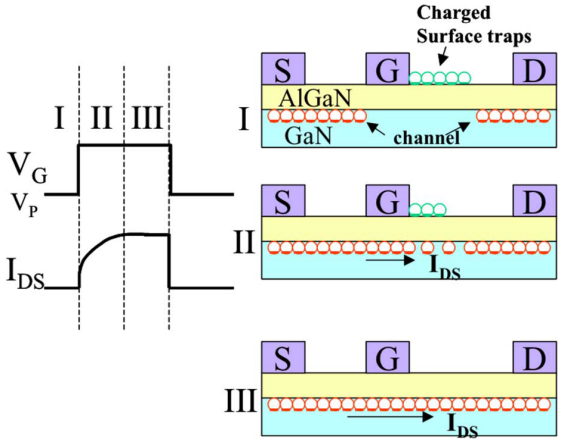


Figure 4.8 Gate-lag process representation in a GaN HEMT, reprinted from [65].

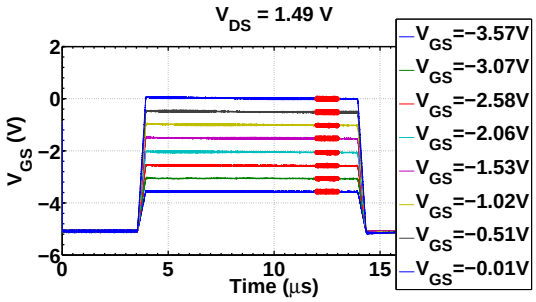
In Figure 4.8 a representation of the pulsed stimulus gate-lag process is depicted. It is divided into three moments. The first moment shows the removal of charge carriers from the conductive channel due to the steady-state electric fields created by drain and gate bias voltages. In the second moment,i.e., when the rising edge of the voltage pulse appears, the carriers are still captured and hence do not contribute to the current in the channel. The release of these carriers is relatively slow and only on the third moment the trapped carriers become available again in the 2DEG.

To analyse the gate-lag phenomena of a 15 W GaN HEMT, the gate pulser described in Chapter 3 was used and the I-V data gathered is shown and discussed in the next paragraphs.

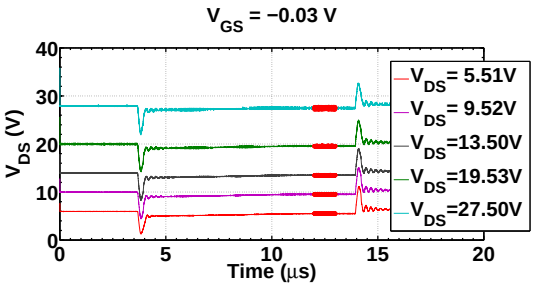
4.3.1 Single-Pulse IV-Curves

Figure 4.9 shows one set of input voltage pulses at the gate and the drain voltages of the HEMT. The latter should stay as much constant as possible since only the gate voltage should be varied in order to isolate the gate-lag effects. A $T_w = 10$ µs pulse width was used with a $T_p = 500$ ms period, which results in a very small duty cycle, $\delta = 0.002$ %, such that thermal

effects are minimized. The "pulsed-off" voltage was $V_{GS_q} = -5$ V to guarantee isothermal conditions for every V_{DS} voltage.



(a) Set of voltage pulses at the gate for $V_{DS} = 1.5$ V.

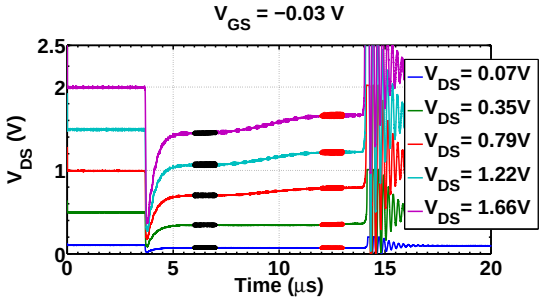


(b) Set of drain voltages corresponding to a voltage pulse from $V_{GS} = -5$ V to $V_{GS} = 0$ V.

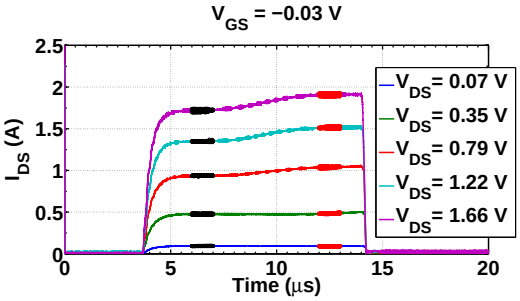
Figure 4.9 Exemplary voltages at gate and drain measured for the I-V curves of a 15W GaN HEMT, the values extracted correspond to the average of the samples with red circles: 13 µs to 14 µs.

During the gate pulse there was a slight deviation during the gate pulse of the drain DC voltage visible in Figure 4.9. This perturbation was caused by the impact of the device and measurement setup parasitics when high I_{DS} currents were generated. However, since the gate and drain voltage are both acquired at the same time of the current, the data used to build the I-V curves are drawn consistently. This is also the reason for the registered 2 decimal digit values of voltages in the legend of Figure 4.9.

Preliminary measurements seemed to reveal discharging of carrier traps at the start of the gate voltage pulse, visible in the non-flat I_{DS} current pulse of Figure 4.10.



(a) Drain voltages, V_{DS}, gate pulsed from $V_{GS} = -5$ V to $V_{GS} = 0$ V.



(b) Drain current pulses, I_{DS}, gate pulsed from $V_{GS} = -5$ V to $V_{GS} = 0$ V.

Figure 4.10 Different sampling windows used during pulsed gate measurements in the triode region. Black circles: 1 µs to 2 µs after the pulse rising edge. Red circles: 8 µs to 9 µs after the pulse rising edge.

This appeared to happen just in the triode region, i.e., for low V_{DS} below the knee voltage and at higher currents, V_{GS} closer to 0 V.

In fact, the apparent charge-carrier trapping is due to the dynamics visible in the V_{DS} voltage within the gate pulse which is more visible in the I_{DS} current when the device is in the linear region. This may have been caused by the parasitics of the DUT,of the measurement setup or both. So, if one draws two I-V curves using samples from two time regions, one at start and another at the end of the gate pulse, if there were trapping effects due to the gate pulse, the resulting curves would differ, which was not the case.

Figure 4.11, shows two I-V curves drawn from data collected at different time regions within the gate pulse, as previously described. There is a rise in V_{DS} and consequently in I_{DS} during the gate pulse but the resulting I-V curves taken on the two different sampling windows still match each other.

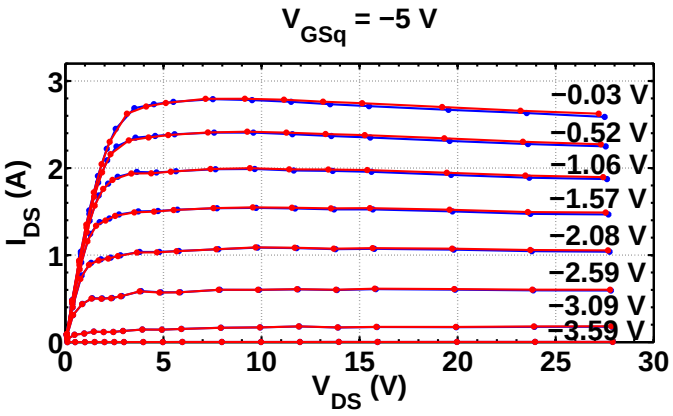


Figure 4.11 I-V curves obtained using the different sampling windows shown in Figure 4.10, blue curves correspond to black dotted sampling window and the red curves to the red dotted window.

Therefore, the impact on the drain current was not caused by any trapping phenomena but by the non-flatness of the drain voltage, whose value should have been constant during the completely flat gate pulse. This is better observed in the linear/triode region where the current is highly dependent on the drain voltage. In the end, this will not affect the shape of the I-V curves and the repeatability of the measurements is guaranteed even though the measured V_{DS} deviates from the wanted V_{DS}, which can be corrected through a simple calibration factor in the drain voltage in a two-pass measurement, one for calibration and another for the actual measurement.

Gate voltage pulses as narrow as 10 µs were used and very small duty cycles leading to an average power of nearly zero. With these conditions and the measurements performed, no

major gate-lag effect could be observed. Unfortunately without a drain pulser there is no possibility of pulsing from quiescent gate voltages, V_{GS_q}, much higher than the threshold voltage of the transistor since the generated drain currents in that situation will become rather high and for increasing values of drain voltages, V_{ds}, the thermal characteristics of the device will become mixed with the trapping effects.

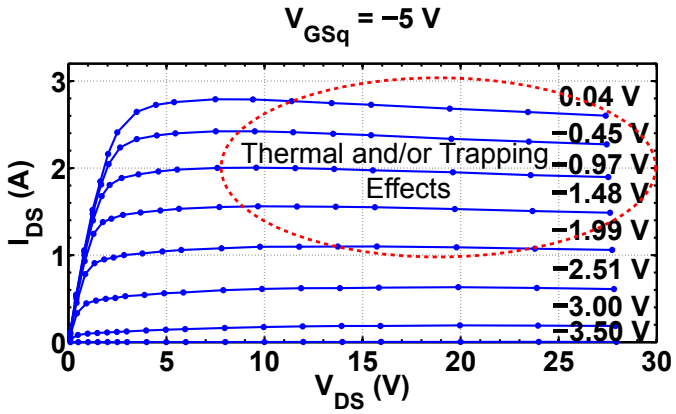


Figure 4.12 Gate pulsed I-V curves obtained, inside the red circle the negative slope of the curves reveal thermal effects within the 5 µ s and/or trapping drain related trapping.

Since one would expect, under RF operation, a positive slope in the I-V curves, corresponding to a positive output resistance, R_{ds}, the negative slope observed, Figure 4.12, must be attributable to thermal and/or trapping effects, being the latter the most probable due to the non-positive slope even at lower V_{DS}/I_{DS} curves, where the dissipated power is lower, and narrow pulses with small duty cycle were used.

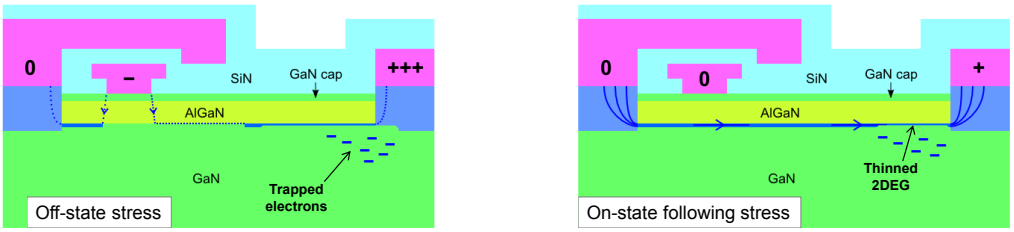
4.4 Pulsed Drain I-V Measurements: Drain-Lag

In a similar way to the gate-lag definition, drain-lag results from the time it takes for the drain current, I_{DS}, to reach its steady state value when a voltage pulse is applied to the drain of the HEMT and the gate voltage remains at a constant value. However, in this case, the observed current is higher immediately after the pulse voltage is applied and will settle down to a lower value after some relatively shot time period, the “trapping” period.

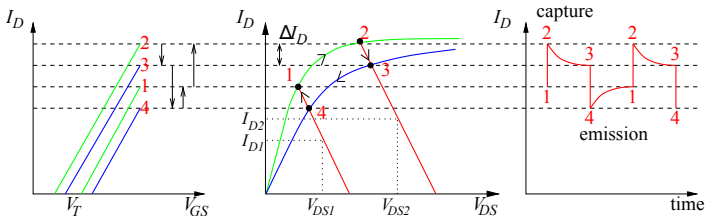
Figure 4.13 shows the typical behaviour of the drain current, I_{ds} when a voltage pulse is applied to the drain. Note the time it takes for the current to reach a steady state when the voltage pulse is high: the time required for the current to rise up to its final high value, $\tau^{dl,trap}$, is relatively short when compared to when it returns to a lower value, $\tau^{dl,detrap}$. This is due to

the very short time constants associated with the “trapping” process.

In order to avoid the relatively longer transient periods resulting from the loading of the drain pulser with the DUT/test-fixture, the pulse widths used were larger than or equal to 10 µs and the corresponding sampling time windows were also chosen to reasonably after the rising edge of the pulses.



(a) Electron trapping due to high electric fields. **(b)** Electrons remain trapped in the bulk states.



(c) Impact on pulsed measurements and the corresponding I-V curves of the capture and emission of electrons.

Figure 4.13 Charge carrier trapping due to high drain voltages resulting in the drain-lag effect, a) and b) reprinted from [11], c) from [66].

4.4.1 Single-Pulse IV-Curves

In Figure 4.14 the drain pulsed voltages, 0.1 V to 28 V, and the corresponding drain currents for a given constant gate voltage, $V_{GS} = 0$ V, are shown. The pulse width used was $T_w = 20$ µs and a pulse repetition period of 500 ms, resulting in a duty cycle of, $\delta = 0.004$ %. The average power being dissipated in the DUT will be,

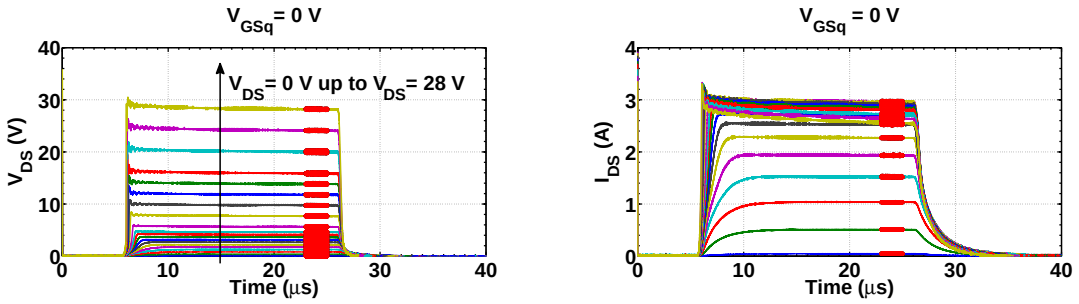
$$P_{d_{avg}} = \frac{T_w}{T_p} \cdot P_{peak} \tag{4.2}$$

$$P_{peak} = V_{max} \cdot I_{max} \tag{4.3}$$

which results in a $P_{d_{avg},max} = 4 \times 10^{-5} \cdot 150$ W$= 6$ mW. Hence, the average power being dissipated is very small which enables at least the removal of the average power induced temperature rise, which means that there may be still thermal effects that are fast enough to be

noticeable inside the time period of the voltage/current pulse, i.e., at or below the µs range.

The IV-curves of a 15 W GaN HEMT were drawn from the pulsed waveforms obtained, as depicted in Figure 4.14, and are shown in Figure 4.15.



(a) Drain voltage pulses, V_{DS}. **(b)** Drain current pulses, I_{DS}.

Figure 4.14 Pulsed V_{DS} and the resulting I_{DS} with the sampling windows used marked with red circles: 17 µs to 19 µs, after the voltage pulse rising edge.

Note again the negative slope, more noticeable on the higher V_{GS} curves, and the higher drain current in the knee region, almost 3 A compared to the 2.8 A on the I-V curves obtained with the gate-pulser. One possible reason for this may be the fact that the 20 µs pulses used in the drain measurements were not long enough to completely fill all the traps, despite that most of them got trapped in the ns scale.

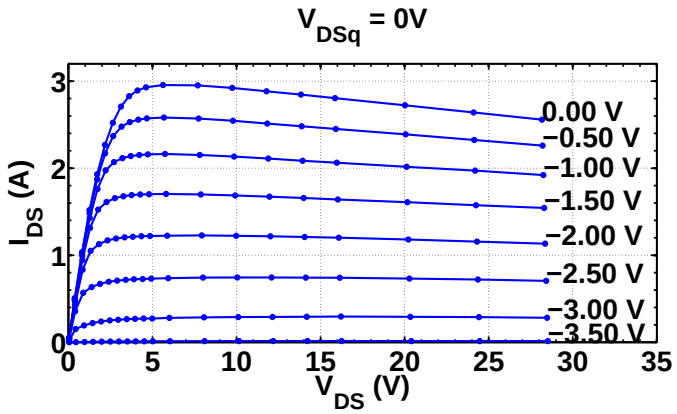


Figure 4.15 Typical I_{DS} and V_{DS} time-domain waveforms resulting from drain-pulsed measurements.

On the raising edge of the voltage pulse, drain-lag itself is rather difficult to observe due to its fast dynamics, on the *ns* scale, which gets mixed with the transient of the acquired waveforms. However, for the higher current/voltage pulses a peak in the I_{DS} current is visible in Figure 4.14 right after the rising edge which almost certainly includes the charging of carriers

traps caused by the high drain voltage pulses. After the pulse falling edge, however, the current collapse caused by trapping phenomena is clearly visible in Figure 4.16. Furthermore, the contrast between the measured trapping and de-trapping processes time constants becomes evident. The latter can take even hundreds of milliseconds, and is possible to measure with the setup when the pulse starts at a non zero quiescent current, I_{DS}, but at reasonably low dissipated powers.

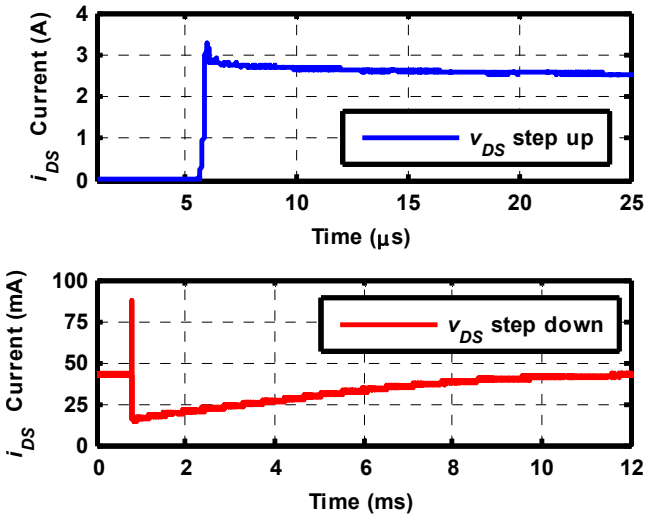


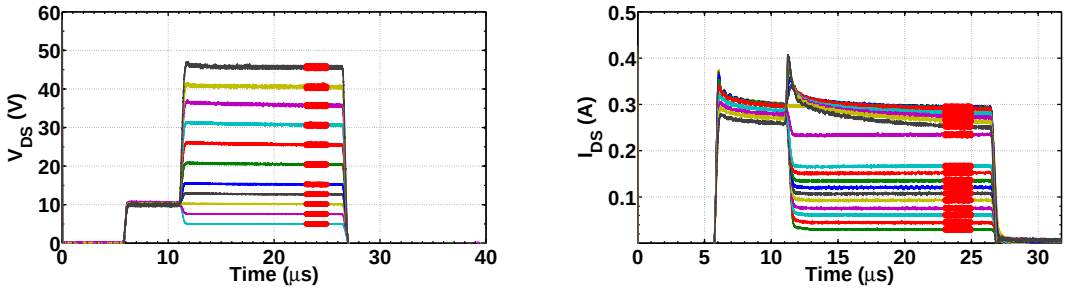
Figure 4.16 Pulsed measurement transients due to trapping of charge carriers in a 15 W GaN HEMT. Blue trace(Step Up): $V_{GSq} = 0$ V, $V_{DSq} = 0$ V and $V_{DS,peak} = 30$ V; Red trace(Step Down): $V_{GSq} = -3.6$ V, $V_{DSq} = 18$ V and $V_{DS,peak} = 28$ V, reprinted from [67].

4.4.2 Double-Pulse - *Quasi-Isodynamic* - IV-curves

To better understand and characterize trapping mechanisms a clever way of using a double pulse measurement was proposed by Santarelli [68]. In this way the charge carriers are forced to get trapped in a controlled manner through the application of a pre-pulse before the typical waveform with a single pulse, called measurement-pulse, is applied and the voltages/currents are acquired.

Figure 4.17 shows the pulsed waveforms applied at the drain, with a pre-pulse of 5 µs immediately followed by a measurement pulse of 15 µs. The pre-pulse should change the state of the traps only if the previous state was due to a lower peak drain voltage, $V_{DS,peak}$. From Figure 4.17 it is also worth noting that the I_{DS} current during the pre-pulse, which was expected to stay at the same level actually decreases with increasing measurement pulses.

This is as visible as the measurement pulse voltage becomes larger than the pre-pulse. The peak current, which is a symptom of carriers getting trapped, also becomes much smaller. This may indicate that even with a period of 500 *m*s some charge carriers remain trapped due to the measurement pulse.



(a) Drain voltage double pulse, V_{DS}.

(b) Drain current double pulse, I_{DS}.

Figure 4.17 Double pulsed V_{DS} and the resulting I_{DS} with the sampling windows used marked with red circles: 17 µs to 19 µs, after the voltage pulse rising edge. The pre-pulse was of $V_{DS} = 10$ V and the gate quiescent voltage was $V_{GSq} = -3$ V.

The resulting I-V curves for a pre-pulse of 10 V and 45 V are depicted in Figure 4.18. Current degradation or collapse is clearly visible but the usually reported *knee-walkout* is less pronounced.

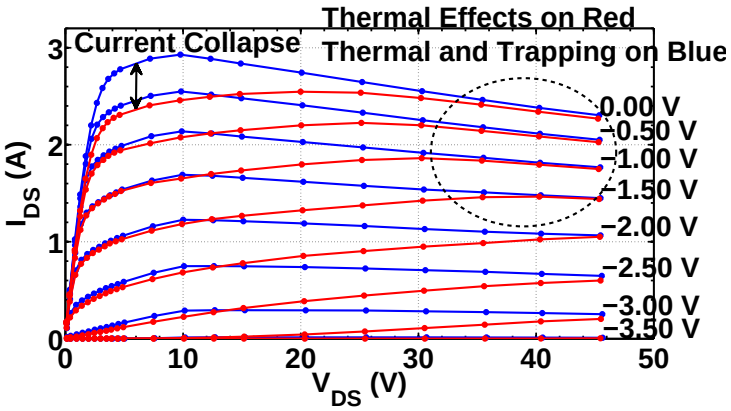


Figure 4.18 I-V curves acquired with the double pulse measurement technique for a 15 W GaN HEMT. Blue trace: $V_{DSq,pre} = 10$ V; Red trace: $V_{GSq,pre} = 45$ V.

On the blue trace, a pre-pulse with 10 V, a combination of thermal and trapping effects is visible at higher V_{DS}/I_{DS}. On the red trace, though, if the pre-pulse of 45 V fully charged the traps the bend visible would be caused by thermal effects. However, there is also the possibility that the pre-pulse is not long enough to fully charge the traps so that even slightly lower

voltages of the measurement pulses, $V_{DS} \leq 45$ V in the case of a pre-pulse of $V_{DS,pre} = 45$ V, will get more charge carriers trapped.

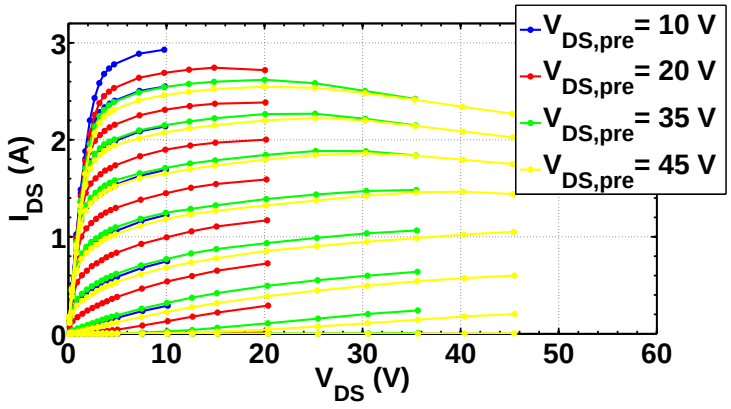


Figure 4.19 I-V curves acquired with the double pulse measurement technique using different pre-set voltage pulses for a 15 W GaN HEMT.

4.5 Modelling Trapping Related LTME

There are different approaches in literature to model trapping related long-term memory effects, both in behavioural [69], or in equivalent circuit compact models [70–72]. When used within an equivalent circuit model they are very often included through one or more equivalent RC circuits whose inputs are the instantaneous gate and drain voltages. These circuits mimic the dynamics of traps and the some voltages across its internal elements usually represent the state of the device in terms of charge carriers trapped. These state variables can then be used as extra input parameters to the non-linear current model.

4.5.1 Including Trapping Related LTME in Compact Models

Trapping effects can be expressed in the instantaneous drain-current dependency as, $i_{DS} = f(v_{GS}, v_{DS}, \vartheta)$, where the additional parameter vector, ϑ, stands for all the parameters related with the trapping and thermal states of the device. However, most modelling approaches include the trapping state parameters within the control voltages v_{GS} and v_{DS}.

In Figure 4.20 one approach to include gate and drain-lag in a compact model of a HEMT is depicted. In this case the current control voltage V_{con} is not equal solely to v_{GS} but it includes

also the gate and drain-lag control voltages according to,

$$V_{con} = V_{gs} + \beta_{gl} V_{gl} + \beta_{dl} V_{dl} \tag{4.4}$$

where the β_{gl} and β_{dl} define the influence of the gate and drain-lag on the V_{con} and ultimately the I_{ds}. Note that the gate-lag is assumed to have equal trapping and de-trapping time constants given by $\tau_{gl} = R_{gl}C_{gl}$ but the drain-lag asymmetric time constants are modelled according to the observed pulsed measurement time-constants through the following expressions resulting from the equivalent circuit,

$$\tau_{dl}^{Trap} = R_b C_b, \qquad \text{with,} \qquad C_b = C_{db} + C_{bs} \tag{4.5}$$

$$\tau_{dl}^{Detrap} = R_{Diode} C_b, \qquad \text{with,} \qquad R_{Diode} = \frac{kT}{q_e I_{diode}} \tag{4.6}$$

which means that one time-constant can be made much longer than the other.

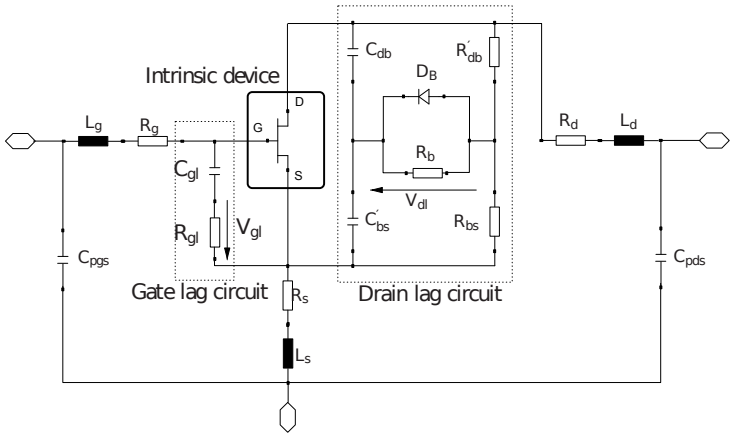


Figure 4.20 Enhanced EEHEMT1 model with circuit elements describing gate and drain lag effects, reprinted from [57].

Some of the parameters are defined before the extraction of the remaining ones such that the impact on the characteristics of the previously developed model that should be maintained are minimal. For instance the sum of the capacitances of C_{db} and C_{bs}, is typically set to be very low, on the order of fF's and the sum of resistances R_{db} and R_{bs} as well as R_b are made very large, MΩ's up to TΩ's. The model is versatile in the sense that it produces transients of either lagging or spiking nature, according to the capacitors and resistors ratios, two factors

are defined,

$$\alpha_c = \frac{C_{bs}}{C_{db}C_{bs}} \qquad \text{and} \qquad \alpha_r = \frac{R_{bs}}{R_{db}R_{bs}} \tag{4.7}$$

if $\alpha_c > \alpha_r$ the generated voltage, V_{dl}, has an overshoot when stepping up but if $\alpha_r > \alpha_c$ it has some lag, when the ratios are equal the resulting voltage pulse becomes squared. To sum up, the time-constants are set by the combination of the diode and resistor R_b with the total capacitance C_b but the type of transient is defined by the relation between the ratios, α_c and α_r. The resistors R_{db} and R_{bs} have minimal impact on the time-constants.

Another approach reported in [70], uses a somewhat similar technique to account for the asymmetrical trapping and de-trapping time-constants associated with drain-lag. This is done by using a diode that only lets the trapping state to be updated faster when the drain voltage brings the trapping state to an higher current degradation state, but is very slow in the de-trapping recovering process, Figure 4.21. That equivalent-circuit model will superimpose an additional dynamic transient depending on trapping effects on the V_{gs} plus its dependence on the V_{ds}, which will produce an effect on the I_{ds} similar to what is observed when the device is measured and characterized at the laboratory.

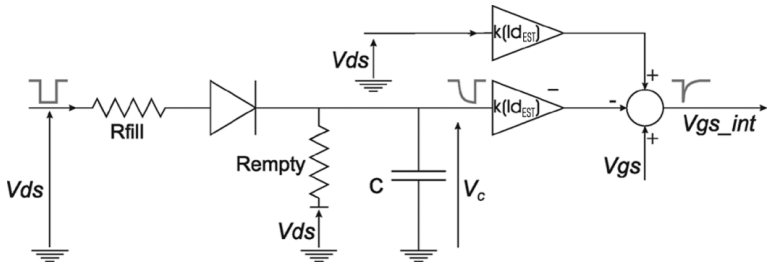


Figure 4.21 Schematic of the drain-lag equivalent-circuit model, reprinted from [70].

The capture time constant is given by,

$$\tau_{fill} \approx R_{fill} \cdot C, \; with \qquad R_{empty} \gg R_{fill} \tag{4.8}$$

and the emission time constant by,

$$\tau_{empty} \approx R_{empty} \cdot C, \; with \qquad R_{empty} \gg R_{fill}. \tag{4.9}$$

The circuit of Figure 4.21 is mathematically expressed as,

$$V_{gs,int} = k(I_{ds,EST}) \cdot [V_{ds} - V_C] + V_{gs} \tag{4.10}$$

with,

$$k(I_{ds,EST}) = k_{rel} \cdot I_{ds,EST}(V_{gs}) \cdot A_{DL} \tag{4.11}$$

where $k(I_{ds,EST})$ is assumed to be linearly or $tanh$ dependent on an estimate of the drain current without trapping effects obtained from a different model, simpler than the full non-linear model, which is said to preserve the model convergence [70]. A_{DL} is a fitting factor in A^{-1}.

4.5.2 Trapping State Dependent Threshold Voltage: V_T Model

Using the double-pulse technique already described several I-V curves were obtained for different trapping state conditions defined by corresponding pre-pulse voltages. Figure 4.22 shows 4 sets of I-V curves for $V_{DS} = 0$ V up to $V_{DS} = 45$ V and for 4 different pre-pulse voltages: 10 V, 20 V, 30 V and 45 V.

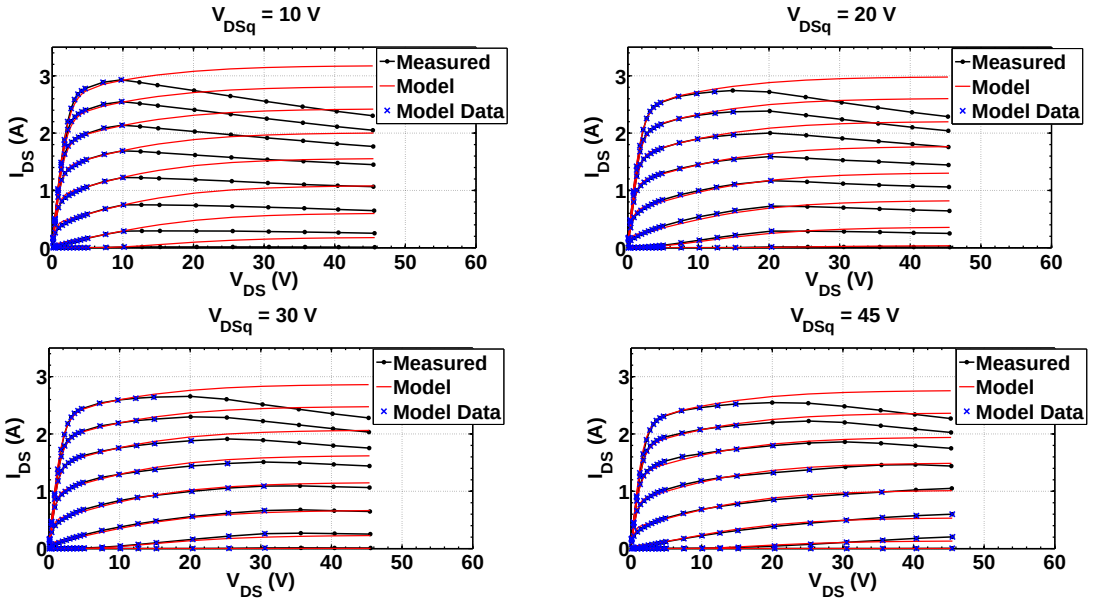


Figure 4.22 Different I-V plots resulting from the double-pulse measurement with different pre-set pulses of: 10 V, 20 V, 30 V and 45 V. Measured data is drawn in black, blue crosses represent the data used for the fitting of the models and the resulting fitted models are drawn in red. The resulting model parameters are forced to be the same in all the models/graphs except the threshold voltage which is allowed to vary for each pre-pulse voltage, i.e., each graph's red traces represent a different model but just due to the different V_T resulting from each fit.

The difference between the I-V curves obtained is huge in terms of current collapse, from

almost 3 A for the pre-pulse of 10 V to 2.5 A for the pre-pulse with 45 V, in the knee region. In order to account for the observed current degradation, the I-V measurements obtained were fitted in MATLAB to the non-linear model briefly described in Chapter 2. Instead of using only one set of I-V curves taken with a voltage pre-pulse of the $V_{DS,bias}$ all the I-V curves for different trapping state conditions were included. In this way, however, extra parameters must be included in the model to account for the big differences between the different I-V curves. What was done was to use several $V_{T,i}$ parameters, one for each different pre-pulsed measurement. The data points used for the fitting of the model are marked as blue crosses in Figure 4.22 and the resulting model curves are traced in red. The choice of the data points used for the non-linear curve fitting was such that the points where thermal effects are mixed with trapping effects were excluded and for each pre-pulse voltage, i.e. trapping state, only the points with V_{DS} below this value were used. This is done due to the asymmetry in the time-constants associated with trapping and de-trapping which will, with the used measurement pulse and pre-pulse time durations, cause the state of the traps to be controlled by the peak drain voltage, V_{DS}. Hence, all the data points greater than the pre-pulse voltage will no longer correspond to a well defined trapping state.

The obtained $V_T(V_{ds,pre})$ are depicted in Figure 4.23. The extra degree of freedom provided by the variation of this parameter can then be included in a device model - Equation (2.15) - as, for example, a $tanh$ analytic functional given by,

$$V_T\left[V_C(t)\right] = V_{T0} + \frac{1}{2}A_{V_T}\left(1 + tanh\left[K_{V_T}\left(V_C(t) - V_{V_T}\right)\right]\right) \tag{4.12}$$

where $V_C(t)$ represents the extracted dynamics of the trapping and de-trapping process.

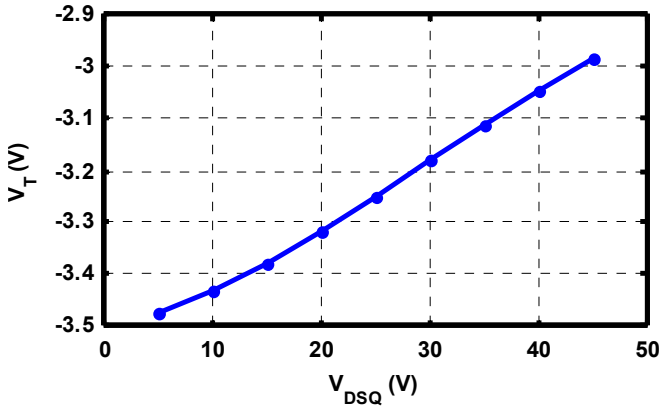


Figure 4.23 Extracted threshold voltage versus the V_{ds} pre-pulse voltage, reprinted from [67].

Chapter 5

Conclusion and Future Work

5.1 Conclusion

The widespread usage of CAD design software made device modelling a fundamental task for the RF industry. Instrumentation is, therefore, intimately related to the modelling process, as, specific instruments/systems are designed and/or commercialized to help characterizing and building accurate models of the devices used in the design of PAs, especially transistors. The main objectives of the work here reported were: the development of a pulsed I-V measurement system such that trapping related LTME of a GaN HEMT could be observed and the characterization of these phenomena.

The development of a pulsed measurement system is not a trivial task. It becomes even more complicated considering the lack of information and details about the specific internal structure of commercially available systems. These pulsed I-V measurement systems are seldom described in literature or by the manufacturers, and only high-level block diagrams are usually presented. Hence, a completely original approach was used to build the gate and drain pulser circuits, in the sense that they were not based on any type of already existing pulser system or circuit. Their design was mainly influenced by several lower-frequency and medium to high power general audio amplifiers circuits. The drain pulser specifications in terms of peak voltage and current made its design much more difficult than the gate-pulser, which was a fairly simple circuit.

The pulsed measurements, obtained from a 15 W GaN DUT with the developed measurement setup revealed, very clearly, the presence of trapping related LTME. The observed drain-lag phenomena was very asymmetric in time due to the very fast trapping of electrons and the very long time needed for them to be released and contribute again to the drain current. This

trapping and releasing processes are a cause of dynamic non-linearities and, therefore, have high impact on the device performance. Thus, accurately modelling the device affected by trapping becomes an even harder task. The gate-lag phenomenon, however, was not clearly observed and its impact was considered to be negligible compared to drain-lag. The relatively recent double-pulse technique was employed, such that quasi-isodynamic measurements were obtained. With those, several trapping state dependent non-linear I-V models of a GaN device were extracted.

5.2 Future Work

There are a couple of tasks that may follow this work. Most of the components used in the pulser circuits, especially the drain-pulser, were specified with a very large margin from their maximum ratings in terms of voltage, current and heat dissipation. Therefore, the drain pulser could be used under more demanding conditions, at least in terms of the peak pulsed voltages and currents.

The pulsed characterization was performed with pulsed voltage excitations at either the gate or the drain. Nevertheless, the usage of the two pulser circuits simultaneously is possible. To do that, the control code developed to manage each setup individually needs to be integrated in one, and the measurement setup assembled accordingly.

After being able to perform pulsed I-V measurements with the gate and drain simultaneously driven, an additional task would be to perform pulsed S-parameter measurements. The accurate realization of this type of measurement is not a trivial task though, and one of its major associated difficulties is what is known as pulse desensitization. This is due to the small duty cycles used, which require higher dynamic range instruments and wider acquisition bandwidths.

Bibliography

[1] V. Nair, "Mobile Wireless Communication Systems and RF Technologies," 2016.

[2] P. Lavrador, T. R. Cunha, P. Cabral, and J. C. Pedro, "The Linearity-Efficiency Compromise," *Microwave Magazine, IEEE*, vol. 11, no. 5, pp. 44–58, 2010.

[3] J. C. Pedro, "The Wonderful World of Nonlinearity : A Distinguished Microwave Lecture on the Modeling and Characterization of RF and Microwave Circuits," *IEEE Microwave Magazine*, vol. 16, no. 9, pp. 22–35, 2015.

[4] H. Chireix, "High Power Outphasing Modulation," *Proceedings of the IRE*, vol. 23, no. 11, pp. 1370–1392, 1935.

[5] W. H. Doherty, "A New High Efficiency Power Amplifier for Modulated Waves," *Proceedings of the IRE*, vol. 24, no. 9, pp. 1163–1182, 1936.

[6] L. Kahn, "Single-Sideband Transmission by Envelope Elimination and Restoration," *Proceedings of the IRE*, vol. 40, no. 7, pp. 803–806, 1952.

[7] F. H. Raab, P. Asbeck, S. Cripps, P. B. Kenington, Z. B. Popovic, N. Pothecary, J. F. Sevic, and N. O. Sokal, "Power ampliïňĄers and transmitters for RF and microwave," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 3, pp. 814–826, 2002.

[8] F. H. Raab, P. Asbeck, S. Cripps, P. B. Kenington, Z. B. Popovic, N. Pothecary, J. F. Sevic, and N. O. Sokal, "RF and Microwave Power Amplifier and Transmitter Technologies - Part 2," *High Frequency Electronics*, no. 5, pp. 22–36, 2003.

[9] D. W. Runton, B. Trabert, J. Shealy, and R. Vetury, "History of GaN: High-power RF gallium nitride (GaN) from infancy to manufacturable process and beyond," *IEEE Microwave Magazine*, vol. 14, no. 3, pp. 82–93, 2013.

[10] J. J. Komiak, "GaN HEMT," *Microwave Magazine, IEEE*, vol. 16, no. 3, pp. 97–105, 2015.

[11] S. Sque, "High-voltage GaN-HEMT devices, simulation and modelling," in *43rd European Solid-State Device Research Conference (ESSDERC 2013), Bucharest, Romania*, 2013.

[12] T. Kikkawa, K. Joshin, and M. Kanamura, "GaN device for highly efficient power amplifiers," *Fujitsu Sci. Tech. J*, vol. 48, no. 1, pp. 40–46, 2012.

[13] P. H. Aaen, J. Pla, and J. Wood, *Modeling and Characterization of RF and Microwave Power FETs*. Cambridge University Press, 2007.

[14] H. Otsuka, T. Oishi, K. Yamanaka, M. Thorsell, K. Andersson, A. Inoue, Y. Hirano, and I. Angelov, "Semi-physical nonlinear circuit model with device/physical parameters for HEMTs," *International Journal of Microwave and Wireless Technologies*, vol. 3, no. 01, pp. 25–33, 2011.

[15] T. Gasseling, "Compact Transistor Models: The Roadmap to First-Pass Amplifier Design Success," *Microwave Journal*, vol. 55, no. 3, pp. 74–86, 2012.

[16] A. R. Alt, D. Marti, and C. R. Bolognesi, "Transistor Modeling: Robust Small-Signal Equivalent Circuit Extraction in Various HEMT Technologies," *Microwave Magazine, IEEE*, vol. 14, no. 4, pp. 83–101, 2013.

[17] "BILT Pulsed IV System Data Sheet GATE & DRAIN Probe heads specifications." *Available at:* `http://www.amcad-engineering.com/IMG/File/IVCAD%20AN%20Overshoots%20PIV%20MT930J.pdf`.

[18] M. Rudolph, C. Fager, and D. E. Root, *Nonlinear transistor model parameter extraction techniques*. Cambridge University Press, 2011.

[19] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 36, pp. 1151–1159, jul 1988.

[20] M. Berroth and R. Bosch, "Broad-band determination of the FET small-signal equivalent circuit," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 38, pp. 891–895, jul 1990.

[21] N. Rorsman, M. Garcia, C. Karlsson, and H. Zirath, "Accurate small-signal modeling of HFET's for millimeter-wave applications," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 44, pp. 432–437, mar 1996.

[22] J. C. Pedro and N. B. Carvalho, *Intermodulation distortion in microwave and wireless circuits*. Artech House, 2003.

[23] P. M. d. S. Cabral, *Modelação não-linear de transistores de potência para RF e microondas*. PhD thesis, Universidade de Aveiro, 2006.

[24] F. De Groote, J. P. Teyssier, T. Gasseling, O. Jardel, and J. Verspecht, "Introduction to measurements for power transistor characterization," *IEEE Microwave Magazine*, vol. 9, no. 3, pp. 70–85, 2008.

[25] J. A. Copeland, "Interpretation of short pulse measurements of electron velocity in GaAs," *Physics Letters A*, vol. 24, no. 1, pp. 9–10, 1967.

[26] M. Paggi, P. H. Williams, and J. M. Borrego, "Nonlinear GaAs MESFET Modeling Using Pulsed Gate Measurements," *IEEE Transactions on Microwave Theory and Techniques*, vol. 36, no. 12, pp. 1593–1597, 1988.

[27] A. Platzker, A. Palevsky, S. Nash, W. Struble, and Y. Tajima, "Characterization of GaAs devices by a versatile pulsed I-V measurement system," in *IEEE International Digest on Microwave Symposium*, pp. 1137–1140, IEEE, 1990.

[28] J. Rodriguez Tellez, B. Stothard, and M. Al-Daas, "Static, pulsed and frequency-dependent current/voltage characteristics of GaAs FETs," *IEE Proceedings - Circuits, Devices and Systems*, vol. 143, no. 3, p. 129, 1996.

[29] A. Parker and D. Root, "Pulse measurements quantify dispersion in PHEMTs," *1998 URSI International Symposium on Signals, Systems, and Electronics. Conference Proceedings (Cat. No.98EX167)*, pp. 444–449, 1998.

[30] "Integrated Pulsed I-V Solutions for Pulsed I-V / RF Measurements ." *Available at:* `http://www.focus-microwaves.com/sites/default/files/IPIV_new.pdf`.

[31] "Agilent Pulsed-IV Parametric Test Solution Selection Guide ." *Available at:* `http://cp.literature.agilent.com/litweb/pdf/5990-3672EN.pdf`.

[32] "AU4850 Pulsed IV/RF Characterization System." *Available at:* `http://www.aurigamicrowave.com/bm.doc/au4850_310714_lo.pdf`.

[33] "Modular Pulsed I-V Solutions for Pulsed I-V / RF Measurements." *Available at:* `http://www.focus-microwaves.com/sites/default/files/MPIV.pdf`.

[34] J. Scott, J. G. Rathmell, A. Parker, and M. Sayed, "Pulsed device measurements and applications," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 44, no. 12, pp. 2718–2723, 1996.

[35] J.-M. Dumas, F. Garat, and D. Lecrosnier, "Development of gate-lag effect on GaAs power MESFETs during aging," *Electronics Letters*, vol. 23, no. 4, pp. 139–141, 1987.

[36] T. M. Barton, C. M. Snowden, J. R. Richardson, and P. H. Ladbrooke, "Narrow pulse measurement of drain characteristics of GaAs MESFETs," *Electronics Letters*, vol. 23, no. 13, pp. 686–687, 1987.

[37] R. Yeats, D. C. D'Avanzo, K. Chan, N. Fernandez, T. W. Taylor, and C. Vogel, "Gate slow transients in GaAs MESFETs-causes, cures, and impact on circuits," in *Electron Devices Meeting, 1988. IEDM '88. Technical Digest., International*, pp. 842–845, 1988.

[38] J. Scottt, A. Parker, and M. Sayedi, "RF, Pulsed-IV, Device Measurement System in VXI," in *Workshop on Applications of Radio Science*, pp. 25–27, 1995.

[39] J.-M. Collantes, C.-Y. Chi, P. C. Canfield, M. Sayed, and R. Quere, "Discrepancies in the transconductance obtained from pulsed S-parameters and pulsed I-V curves of PHEMT devices," in *Microwave Conference Proceedings, 1997. APMC '97, 1997 Asia-Pacific*, pp. 505–508 vol.2, 1997.

[40] R. J. Donarski, A. K. Jastrzebski, and J. E. Barnaby, "Pulsed I-V and temperature measurement system for characterisation of microwave FETs," in *Microwave Symposium Digest, 1995., IEEE MTT-S International*, pp. 1523–1526 vol.3, 1995.

[41] V. Cuoco, M. de Kok, M. Heijden, and L. C. N. de Vreede, "Isothermal Non-Linear Device Characterization," in *ARFTG Conference Digest-Fall, 58th*, vol. 40, pp. 1–4, nov 2001.

[42] A. Santarelli, R. Cignani, D. Niessen, S. D'Angelo, P. A. Traverso, and F. Filicori, "Characterization of GaN and GaAs FETs through a new pulsed measurement system," in *Microwave Integrated Circuits Conference (EuMIC), 2011 European*, pp. 1–176, 2011.

[43] C. Baylis, L. Dunleavy, and W. Clausen, "Design of bias tees for a pulsed-bias, pulsed-RF test system using accurate component models," *Microwave journal*, vol. 49, no. 10, 2006.

[44] "BIAS TEES, Pulsed. Aeroflex / Inmet , Inc." *Available at:* `http://ams.aeroflex.com/inmet/pdfiles/8860S.PDF`.

[45] P. Roblin, *Nonlinear RF circuits and nonlinear vector network analyzers: interactive measurement and design techniques.* Cambridge University Press, 2011.

[46] J. P. Martins, N. B. Carvalho, and J. C. Pedro, "A Figure of Merit for the Evaluation of Long Term Memory Effects in RF Power Amplifiers," in *Microwave Symposium Digest, 2006. IEEE MTT-S International*, pp. 1109–1112, 2006.

[47] W. Bosch and G. Gatti, "Measurement and Simulation of Memory Effects in Predistortion Linearizers," vol. 37, no. 12, pp. 1885–1890, 1989.

[48] L. O. Chua, C. A. Desoer, and E. S. Kuh, *Linear and Nonlinear Circuits.* McGraw-Hill. Inc., 1987.

[49] J. Wood, "Pre-Distortion Techniques for RF Power Amplifiers," *Besser Associates Course on RF Power Amplifier Digital Pre-Distortion (DPD) & Behavioral Modeling*, 2011.

[50] J. Verspecht, "Everything You Always Wanted To Know About," *in IEEE MTT-S Int. Microwave Workshop 'Introducing New Concepts in Nonlinear Network Design', Seattle, WA*, 2002.

[51] N. B. De Carvalho, "Large- and small-signal imd behavior of microwave power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 12, pp. 2364–2374, 1999.

[52] J. Wood, M. LeFevre, D. Runton, J. C. Nanan, B. H. Noori, and P. H. Aaen, "Envelope-domain time series (ET) behavioral model of a Doherty RF power amplifier for system design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 8, pp. 3163–3171, 2006.

[53] G. Riley, "Accounting for Dynamic Behavior in Fet Device Models," *Microwave Journal*, vol. 54, no. 7, pp. 80–86, 2011.

[54] M. Khan, J. N. Kuznia, J. M. Van Hove, N. Pan, and J. Carter, "Observation of a two-dimensional electron gas in low pressure metalorganic chemical vapor deposited GaN/Al-GaN heterojunctions," *Applied Physics Letters*, vol. 60, pp. 3027–3029, jun 1992.

[55] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors," *Applied Physics Letters*, vol. 77, pp. 250–252, jul 2000.

[56] U. K. Mishra, P. Parikh, and Y.-F. Wu, "AlGaN/GaN HEMTs-an overview of device operation and applications," *Proceedings of the IEEE*, vol. 90, pp. 1022–1031, jun 2002.

[57] S. Chalermwisutkul, *Large Signal Modeling of GaN HEMTs for UMTS Base Station Power Amplifier Design Taking Into Account Memory Effects*. Phd thesis, Rheinisch-Westfälischen Technischen Hochschule Aachen, 2007.

[58] U. K. Mishra, L. Shen, T. E. Kazior, and Y. F. Wu, "GaN-based RF power devices and amplifiers," *Proceedings of the IEEE*, vol. 96, no. 2, pp. 287–305, 2008.

[59] F. Filicori, G. Vannini, A. Mediavilla, and A. Tazon, "Modelling of deviations between static and dynamic drain characteristics in GaAs FETs," in *Microwave Conference, 1993. 23rd European*, pp. 454–457, 1993.

[60] F. Filicori, G. Vannini, A. Santarelli, A. M. Sanchez, A. Tazon, and Y. Newport, "Empirical modeling of low-frequency dispersive effects due to traps and thermal phenomena in III-V FET's," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 43, no. 12, pp. 2972–2981, 1995.

[61] P. Javorka, *Fabrication and Characterization of AlGaN / GaN High Electron Mobility Transistors*. Phd thesis, Rheinisch-Westfälischen Technischen Hochschule Aachen, 2004.

[62] P. McGovern, J. Benedikt, P. J. Tasker, J. Powell, K. P. Hilton, J. L. Glasper, R. S. Balmer, T. Martin, and M. J. Uren, "Analysis of DC-RF dispersion in AlGaN/GaN HFETs using pulsed I-V and time-domain waveform measurements," in *IEEE MTT-S International Microwave Symposium Digest, 2005.*, pp. 4–pp., 2005.

[63] J.-C. Nallatamby, R. Sommet, S. Laurent, M. Prigent, R. Quere, and O. Jardel, "A Microwave Modeling Oxymoron?: Low-Frequency Measurements for Microwave Device Modeling," *Microwave Magazine, IEEE*, vol. 15, no. 4, pp. 92–107, 2014.

[64] S. C. Binari, P. B. Klein, and T. E. Kazior, "Trapping effects in GaN and SiC microwave FETs," *Proceedings of the IEEE*, vol. 90, pp. 1048–1058, jun 2002.

[65] A. Kalavagunta, M. Silvestri, M. J. Beck, S. K. Dixit, R. D. Schrimpf, R. A. Reed, D. M. Fleetwood, L. Shen, and U. K. Mishra, "Impact of proton irradiation-induced bulk defects on gate-lag in GaN HEMTs," *IEEE Transactions on Nuclear Science*, vol. 56, no. 6, pp. 3192–3195, 2009.

[66] S. Joo Doo, *New pulsed-iv pulsed-rf measurement techniques for characterizing power fets for pulsed-rf power amplifier design.* Phd thesis, The Ohio State University, 2008.

[67] L. C. Nunes, J. M. Gomes, P. M. Cabral, and J. C. Pedro, "A new nonlinear model extraction methodology for GaN HEMTs subject to trapping effects," in *2015 IEEE MTT-S International Microwave Symposium*, pp. 1–4, 2015.

[68] A. Santarelli, R. Cignani, G. P. Gibiino, D. Niessen, P. A. Traverso, C. Florian, D. M. M. P. Schreurs, and F. Filicori, "A Double-Pulse Technique for the Dynamic I/V Characterization of GaN FETs," *IEEE Microwave and Wireless Components Letters*, vol. 24, pp. 132–134, feb 2014.

[69] J. C. Pedro, P. M. Cabral, T. R. Cunha, and P. M. Lavrador, "A Multiple Time-Scale Power Amplifier Behavioral Model for Linearity and Efficiency Calculations," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 61, pp. 606–615, jan 2013.

[70] O. Jardel, F. De Groote, T. Reveyrand, J.-C. Jacquet, C. Charbonniaud, J.-P. Teyssier, D. Floriot, and R. Quere, "An Electrothermal Model for AlGaN/GaN Power HEMTs Including Trapping Effects to Improve Large-Signal Simulation Results on High VSWR," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 55, no. 12, pp. 2660–2669, 2007.

[71] O. Jardel, F. De Groote, C. Charbonniaud, T. Reveyrand, J.-P. Teyssier, R. Quere, and D. Floriot, "A Drain-Lag Model for AlGaN/GaN Power HEMTs," in *Microwave Symposium, 2007. IEEE/MTT-S International*, pp. 601–604, 2007.

[72] J. B. King and T. J. Brazil, "Equivalent circuit GaN HEMT model accounting for gate-lag and drain-lag transient effects," in *2012 IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications*, pp. 93–96, IEEE, jan 2012.

Appendix A

Agilent ADS Simulation Schematics

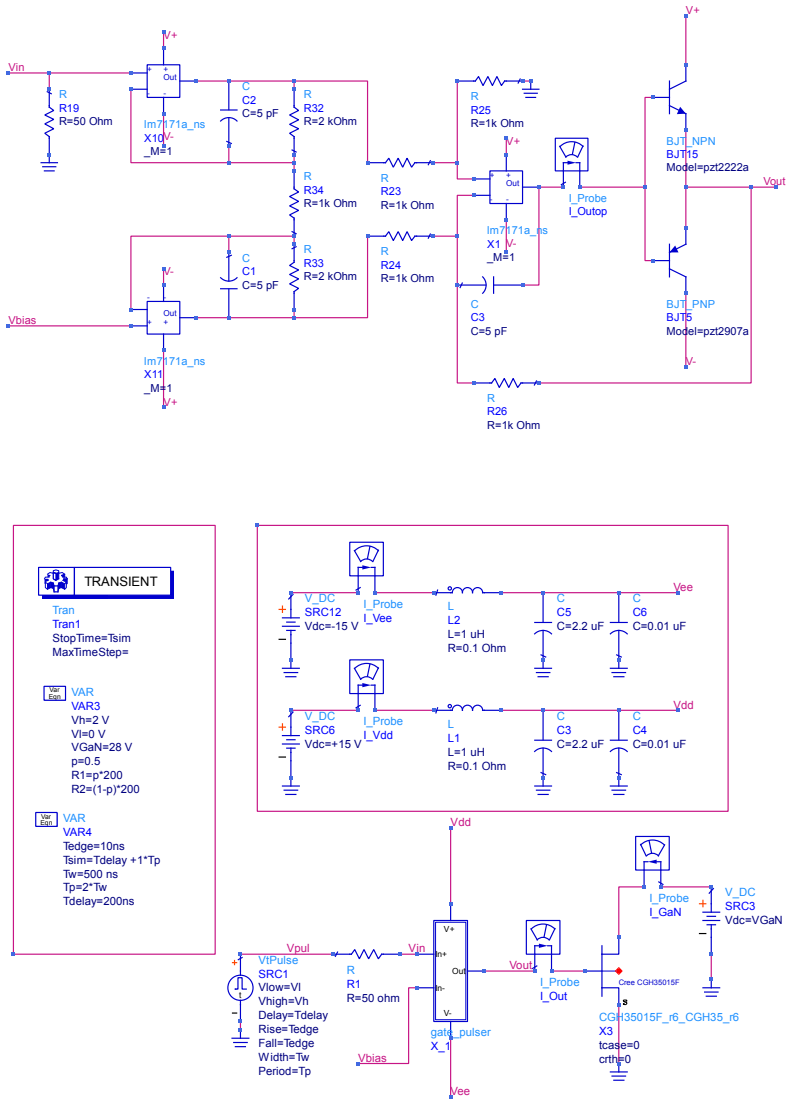


Figure A.1 Gate pulser *Agilent ADS* simulation schematic. The blocks corresponding to the device models used were obtained from the manufacturer.

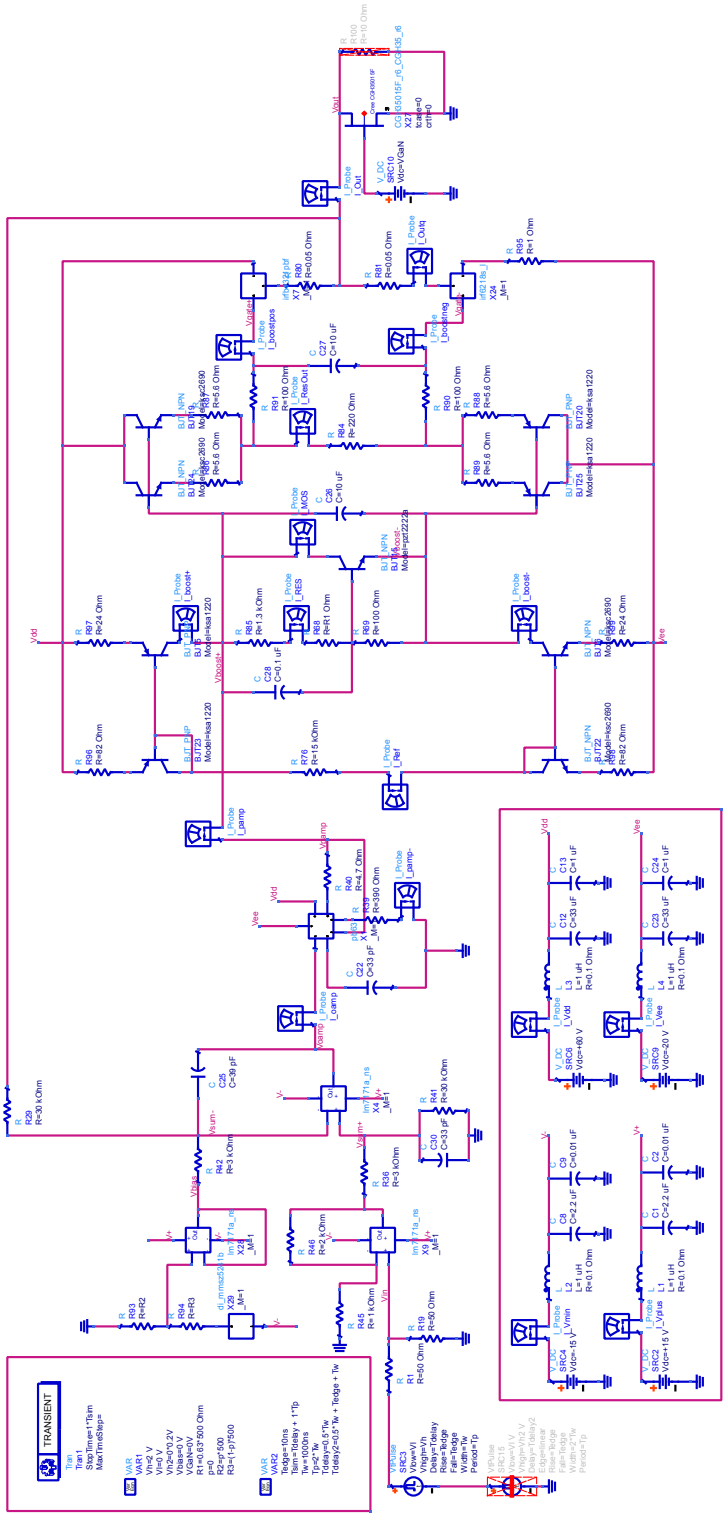
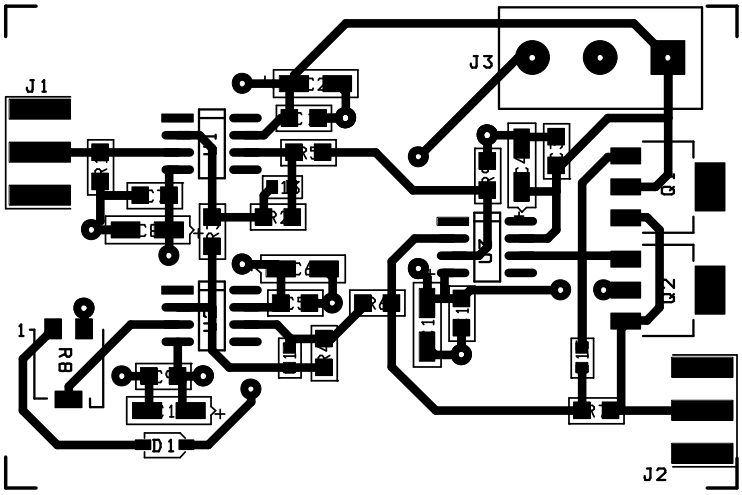


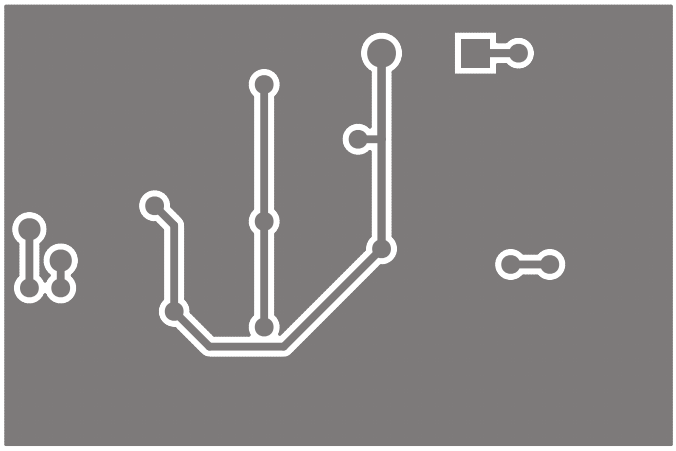
Figure A.2 Drain pulser *Agilent ADS* simulation schematic. The blocks corresponding to the device models used were obtained from the manufacturer.

Appendix B

PCB Layouts

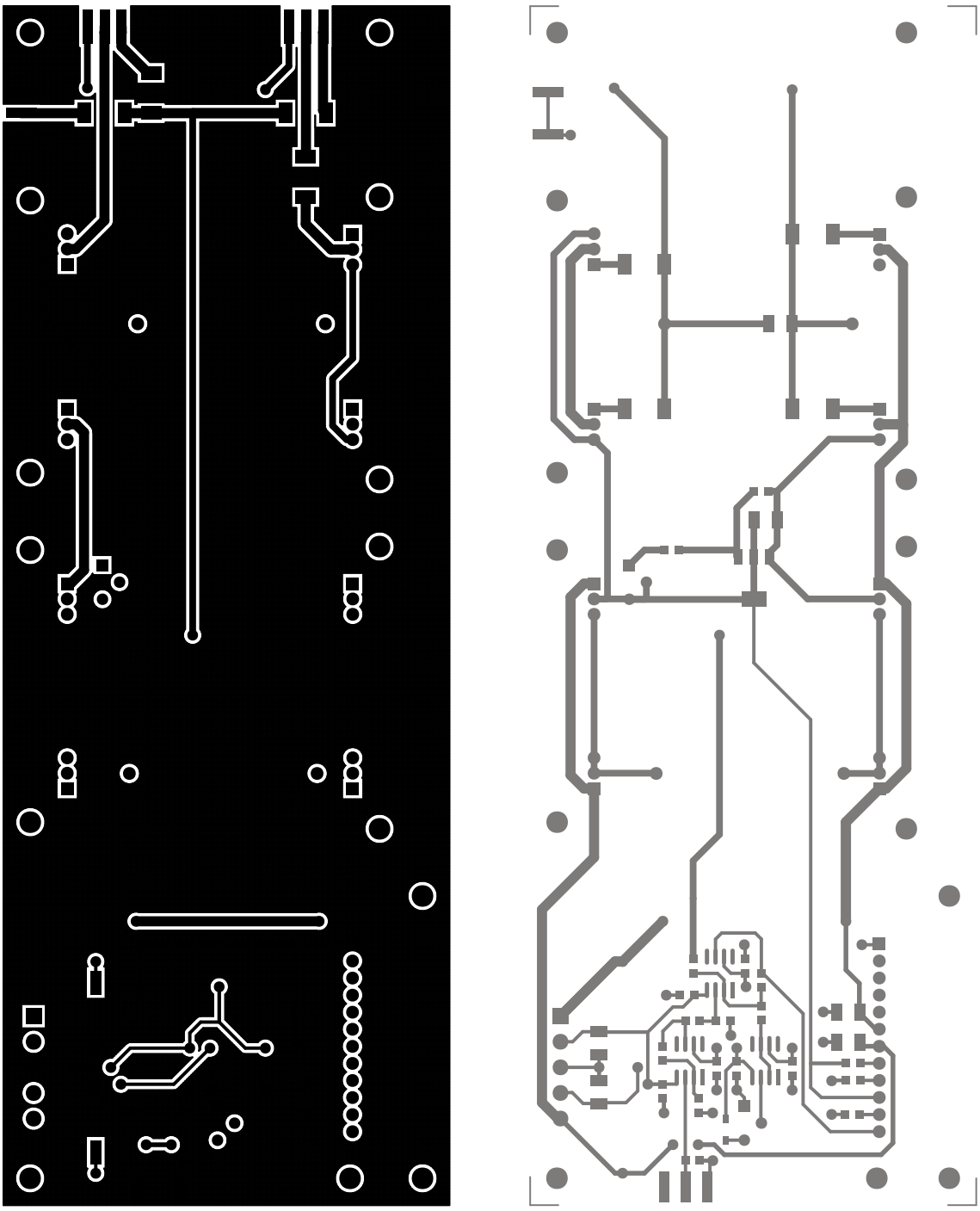


(a) Top layer.



(b) Bottom layer.

Figure B.1 Layout of the gate pulser PCB implementation on an FR-4 substrate.



(a) Top layer.

(b) Bottom layer.

Figure B.2 Layout of the drain pulser PCB implementation on an FR-4 substrate.